Dead-time effect analysis of a three-phase dual-active bridge DC/DC converter

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Abstract: The dead-time effect is observed in the three-phase dual-active bridge (DAB) DC/DC converter. The occurrence of the dead-time effect depends on the relationship of the switching frequency, the phase shift value, the dead-time value and the equivalent conversion ratio. The dead-time effect may have a significant impact on the converter performance when high switching frequency, wide input and output voltage range or wide operation power range are required. Therefore, comprehensive research of the dead-time effect is essential to improve the design of the three-phase DAB converter over a wide operation range. In this study, all the cases of the dead-time effect in the three-phase DAB converter are analysed in terms of the buck, boost, and matching states. The expressions of the transmission power, constraint conditions, and key time of the dead-time effect are derived for each state. The operation waveforms of the dead-time effect are also presented to better understand the dead-time effect. Finally, the analysis is verified by both simulation and experimental results.

1 Introduction

Dual-active bridge (DAB) converters are attracting significant attention in several applications due to their features such as galvanic isolation, bidirectional operation, high power density, and high efficiency [1]. Compared with full-bridge DC–DC converters, DAB converters use active switches on both sides to achieve bidirectional operation. With proper selection of the dead-time value, the DAB topology can achieve natural zero voltage switching (ZVS) on both sides by using the phase shift control. The single-phase DAB converter is widely studied for decades. An active filter auxiliary power module based on DAB topology is proposed in a vehicle application in [2]. A current-fed DAB converter is applied in the grid-tied photovoltaic (PV) system [3]. A detailed overall study of a DAB for the bidirectional DC/DC converter, including the design and small-signal model of the single-phase DAB, can be found in [4]. Two design approaches based on increasing ZVS operation range and improving efficiency at full load are proposed in [5]. Typically, the single-phase DAB converter suffers from its large capacitor banks on both input side and output side, which are needed to filter out the current ripples [6]. In comparison, the three-phase DAB converter, which can reduce the required capacitance significantly, is a promising alternative to the single-phase DAB in high-power applications [7–9]. According to [6], the capacitance on both sides of the three-phase DAB converter is around one third of that in the single-phase DAB converter. Besides, the three-phase DAB converter is more efficient due to lower backflow power compared to the single-phase DAB converter with similar power rating.

Since the power switches have turn-on and turn-off delay time, a DC path exists between the supply lines if the ‘on’ states of the two switching devices overlap in half-bridge or full-bridge applications. This is called ‘cross conduction’ and cause immediate failure. A dead time will be introduced as the period at which both devices are off to prevent the cross conduction [10]. So the dead time is usually designed for the turn-on and turn-off delay time. On the other hand, the dead time in DAB is also designed to ensure ZVS which depends on the oscillation time caused by the leakage inductance and the switch's stray capacitance [11]. However, when the dead time is introduced, the dead band effect and the phase shift error in the single-phase DAB converter, was analysed for the short-time-scale transient processes in [12]. The operation and design of the single-phase DAB converter are studied in [13] and the dead-time effect of the primary H-bridge is analysed. Based on the experimental tests, the internal power transfer, phase drift, and low system efficiency are observed for the single-phase DAB converter in [14]. A new power flow model over a short-time scale is proposed that incorporates additional parameters, including the power semiconductor voltage loss and dead time in [14]. Other dead-time effect phenomena, such as voltage polarity reversal and voltage sag, are observed [15] and a comprehensive theoretical analysis and experimental verification are studied for single-phase DAB converter. Only one case of the dead-time effect in three-phase DAB converter is also observed in [11]. This paper provides the comprehensive theoretical analysis for all the possible cases of the dead-time effect in three-phase DAB converter. In an effort to minimise the influence of the dead-time effect, dead-time compensation can be applied in the controller loop [16], most of which rely on the analytic closed-form expressions of the dead-time effect. Therefore, the dead-time analysis presented in this paper provides an insight into the dead-time compensation of the three-phase DAB converter. In our future work, we are going to investigate the dead-time compensation schemes based on the analysis we did in this paper.

High switching frequency is desired for modern power converters because it can help shrink the size of the bulk passive components in the system [17]. Wide bandgap devices, like silicon carbide (SiC) and gallium nitride (GaN), enables the high switching frequency in the power electronics because of their low switching loss [18]. The dead-time effect is essential to design a DAB converter with very high switching frequency [19]. On the other hand, wide operation condition, input/output voltage and power, are required by power converters, like battery-interface DC/DC converters. However, the impact of the dead-time effect is more obvious when high switching frequency and wide operation range are required. Thus the comprehensive research of the dead-time effect is essential for the implementation of the three-phase DAB.

This paper aims to improve the design of the dead-time of the three-phase DAB at different operating conditions by comprehensively analyse the dead-time effect in terms of the conversion ratio and phase shift value. The organisation of this...
Section 1 introduces the research topic of the DAB topology and the motivation of the work. Section 2 describes the dead-time effect in the three-phase DAB topology. Section 3 presents the detailed analysis of the dead-time effect in different operation mode especially the operation waveforms and expression equations. In Section 4, experimental results are presented to validate the simulation results. Finally, Section 5 concludes the findings and summarises contributions of this paper.

2 Dead-time effect of the three-phase DAB converter

2.1 Conventional operation of the three-phase DAB DC/DC converter

A typical three-phase DAB DC/DC converter is illustrated in Fig. 1. With the single-phase-shift (SPS) control method, the operation principle of the three-phase DAB converter is similar to that of the single-phase converter. Each phase conducts 120° in turn while the phase shift is controlled between two sides of the converter to produce a voltage difference across the leakage inductance of the transformers. The basic idea is to utilise the voltage difference across the inductor to induce the current flow and, thus, the power can be delivered from one side to the other side. Three individual transformers with the same parameters which are connected in Y type are more promising, as shown in Fig. 1, because it adds more flexibility to the converter. For example, the performance evaluation for three phase DAB converter with different transformer configuration is proposed in [20]. The index, which will be used in this paper is summarised in Table 1.

<table>
<thead>
<tr>
<th>Index symbol</th>
<th>Index</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_i$</td>
<td>input DC voltage on the primary side</td>
</tr>
<tr>
<td>$V_o$</td>
<td>output DC voltage on the secondary side</td>
</tr>
<tr>
<td>$n$</td>
<td>turn ratio of the transformer</td>
</tr>
<tr>
<td>$M$</td>
<td>effective turn ration $M = V_o/nV_i$, where $n$ represents the turn ratio of the transformer</td>
</tr>
<tr>
<td>$\phi$</td>
<td>phase shift value in rad</td>
</tr>
<tr>
<td>$L$</td>
<td>leakage inductance of the transformer</td>
</tr>
<tr>
<td>$D$</td>
<td>dead-time value in rad</td>
</tr>
<tr>
<td>$\omega$</td>
<td>converter switching frequency in rad</td>
</tr>
</tbody>
</table>

The biggest advantage of the DAB topology is that all the switches can operate in turn-on ZVS which makes it highly efficient. However, in order to achieve soft-switching, sufficient dead time should be given so that the switch voltage drop to zero before the switch is turned on [11]. The traditional operation waveforms of the three-phase DAB converter with SPS control with $\phi \in [0, \pi/3]$ can be found in Fig. 2a, where $v_{HA}$ and $v_{HA}$ represent the voltages across the switches S1 and Q1, respectively, $v_{AO}$ and $v_{AO}$ represent the phase voltages of the transformer A and

![Fig. 1 Topology of the three-phase DAB converter](image)

![Fig. 2 Operation waveforms](image)

Fig. 1 Topology of the three-phase DAB converter

Fig. 2 Operation waveforms

(a) Conventional, (b) Dead-time effect (simulation condition: dead-time in rad is 0.70; phase shift in rad is 0.48)

$i_A$ represents the current going through transformer A. In this paper, we define the current going through the metal–oxide–semiconductor field-effect transistor (MOSFET) switch from source to drain as negative and otherwise as positive. The upper graph in Fig. 2a shows the voltage across the switch. The lower graph in Fig. 2a shows the voltage of the phase A and the current of the phase A transformer. When the current going through the switch is negative during the dead-time interval, the body diode of the switch is conducting then the voltage across the switch will drop to zero before the switch is turned on. Thus, the turn on ZVS can be achieved. A lower limit of the dead time has to be designed to ensure ZVS. If the dead time is a relatively large value, the dead-time effect will happen.

2.2 Dead-time effect phenomena in three-phase DAB converter

In [15], the voltage polarity reversal, voltage sage and phase shift are found in single-phase DAB converter. They all exist in the three-phase DAB converter.

The voltage polarity reversal as a typical dead-time effect of the three-phase DAB converter is still observed in Fig. 2b. In the upper waveforms of Fig. 2b, a voltage pulse during the switch turning on and voltage sag during the switch turning off can be observed. This
phenomenon is a so-called voltage polarity reversal which can be also seen in the single-phase DAB converter [15]. When the current going through the switch is positive during the dead-time interval, the body diode of the other switch of the same leg will be conducted and the voltage across the switch will be the DC-bus voltage. Thus the so-called voltage polarity reversal happens. When the current going through the switch is zero during the dead time, the voltage sag will happen where the voltage value should be depend on the voltage of other legs. The dead-time effect of the single-phase DAB converter is straightforward it’s a full-bridge topology. However, the analysis of the three-phase DAB will be more complicated because its three half-bridge topologies will cause the voltage difference across the inductor depending on all the voltage shape of the three legs.

The transmission power of the conventional case \( (\varphi \in [0, \pi/3]) \) and dead-time effect case are illustrated in Fig. 3 and can be calculated as

\[
P = \frac{MV_0^2}{2} \left( \frac{2}{3} - \frac{\varphi}{2\pi} \right)
\]  

(1)

The input and output voltages of interest are 34 and 180 V, respectively. The turn ratio of the applied transformers is 1:6. The different trend of the power curve before and after \( \pi/3 \) is caused by the different operation modes of the three-phase DAB converter \( (\varphi \in [0, \pi/3] \) and \( \varphi \in [\pi/3, 2\pi/3] \) [6]. The green dot curve represents the simulation power results with dead-time as 0.35 rad. Based on the observation of Fig. 3, the transmission power is the same as the conventional case for larger phase shift value. However, at lower phase shift value, the transmission power is quite non-linear with the phase shift value. This is because of the voltage distortion due to voltage sag and voltage reversal. At first, the transmission power is lower than a conventional operation. Then the power at a lower phase shift value is kind of “saturated” where lower transmission power will not be achieved. This may cause malfunction of the converter. Thus, the dead-time effect should draw enough attention when designing the converter with a wide operation range. Moreover, the comprehensive analysis of the dead-time effect is needed.

3 Dead-time effect analysis details of the three-phase DAB converter

The comprehensive analysis of the dead-time effect will be shown in this section. Since the phase voltage of the transformer highly depends on the equivalent conversion ratio \( M \), all of the dead-time effects can be categorised into three operational states: boost \( (M > 1) \), buck \( (M < 1) \) and matching \( (M = 1) \). The detailed analysis of the operation waveforms can be found. The constrain equations, the transmission power and key characterising timing can also be found. Due to the symmetry of the three-phase DAB topology, only 60° of the waveform in Phase A is analysed as an example and the other analysis can refer to it. The range of the interested dead-time is \( 0 \sim \pi/3 \) because of larger dead-time results in too small conduction time. The phase shift value range is \( 0 \sim 2\pi/3 \) in this work because the larger phase shift produces too much backflow power [6].

3.1 Boost state \( (M > 1) \)

3.1.1 Mode A1: When \( 0 \leq \varphi < D \) and \( 0 \leq \varphi < t_{so} \), the operation waveforms are illustrated in Fig. 4a where \( t_{so} \) represents the time when the current going through the transformer, \( t_{so} \), equals to zero in the half period.

At \( t_{so} \), the switch \( S_1 \) is turned ON. The equivalent circuit is as shown in Fig. 5a. During the interval between \( t_s \) and \( t_{so} \), \( Q_1 \) and \( Q_3 \) are turned OFF due to the dead time. Besides, there is no current going through \( T_A \), their body diode is not conducting. On the other hand, \( S_1, S_3 \) and \( S_4 \) are turned ON so the voltage \( V_{oA} \) can be easily derived from \( V_o/3 \) using the basic circuit theory.

Based on the basic circuit theory, the expression equations describing the relationship between the voltages are summarised as

\[
\begin{align*}
V_{oA} &= nV_o/3 \\
V_{oA} + V_{ih} &= V_{oA} \\
V_{oA} &= V_{o} \\
V_{oA} + V_{oh} + V_{oA} &= 0 \\
V_{oA} &= (3V_o - nV_o)/6 \\
V_{oA} &= (3V_o + nV_o)/6 \\
V_{ih} &= (V_o - nV_o)/2
\end{align*}
\]

(2)

The voltage can be derived as (3) by solving (2)

\[
\begin{align*}
V_{oA} &= nV_o/3 \\
V_{oA} &= (3V_o - nV_o)/6 \\
V_{oA} &= (3V_o + nV_o)/6 \\
V_{ih} &= (V_o - nV_o)/2
\end{align*}
\]

(3)

From \( t_s \) to \( t_{so} \), \( Q_1 \) begins to conduct. On the primary side, although \( S_1 \) is turned OFF, its body diode is still conducting because \( i_C \) is negative as shown in Fig. 5b. Based on the operation of the converter, the voltage \( V_{oA} \) and \( V_{o} \) can be derived as \( V_o/3 \) and \( V_o/3 \). Thus, the voltage across \( L_A \) is \( (nV_{iA} - V_o)/3n \). The voltage is negative because of the boost state \( (M > 1) \). This voltage will cause \( i_{so} \) to increase linearly in the negative direction.

During the interval between \( t_{so} \) and \( t_{so} \), the primary side of the converter remains the same. At \( t_{so} \), \( Q_3 \) is turned OFF. Due to the leakage inductance in the transformer, the current \( i_C \) cannot change instantaneously at that moment. Thus the negative direction of \( i_C \) forces the body diode of \( Q_3 \) to conduct as shown in Fig. 5c. The voltage across \( L_C \) is \( (nV_{iA} - V_o)/3n \) resulting in the current going through it to decrease in the negative direction. \( i_{sc} \) ends up to zero at \( t_s \).

Since \( i_C \) is zero at \( t_s \), the body diodes of \( S_3 \) and \( Q_4 \) have not conducted anymore as shown in Fig. 5d. Since there is no current in the leakage inductor, \( V_{oA} \) and \( V_{o} \) are zero. The voltages \( V_{oB} \) and \( V_{oC} \) equal to \( V_i/2 \) and \( V_i/2 \), respectively. Based on KVL, \( V_{oA} \) and \( V_{oB} \) are \( V_{i}/2 \) and \( V_{i}/2 \), respectively. The rest of the waveform can be analysed based on the similar analyse procedure for the phases B and C. For example, the interval \( t_s \sim t_s \) in Phase A can be analysed following the same step analysing interval \( t_s \sim t_s \) for Phase C. Then the voltage is derived as \( V_{oA} \) \( = (3V_o + 3V_o)/6 \) according to (3).

After observing the operation waveform, ZCS can be achieved for the primary side switches during turning on and off while ZVS can be achieved for the secondary side switches during turning on. This mode can be utilised to increase efficiency when ZVS is lost in light load condition of the regular modulation. Although the transmission power here is negative, we can see this mode as a Buck state with positive transmission power.
Table 2 summarises the constraint conditions and the corresponding transmission power expressions. Considering the length of the paper, the derivations are not shown here. The time of the zero current in Fig. 4.41 is derived from

\[ t_0 = \frac{2(2m + 3D - 2nM)}{3(M + 1)} \]  \hspace{1cm} (4)

**3.1.2 Mode A2:** If $0 \leq \phi < D$ and $0 \leq t_0 < \phi$, the operation waveforms are illustrated in Fig. 4.42.

Since $0 \leq t_0 < \phi$ the Mode A2 does not have the zero $V_{AO}$ situation. At $t_0$, $S_1$ is turned ON. During the time interval $t_0$, the current $i_A$ is positive as shown in Fig. 5. Although $Q_1$ is turned OFF, the body diode is conducting because of the positive current $i_A$. Based on the operation condition, the voltage across $L_A$ is $(nV_i - V_o)/3n$ which is negative due to $M > 1$. Hence, the current $i_A$ decreases linearly in the positive direction, then it ends up to zero at $t_0$. The analysis of the intervals $t_0$, $A_2$ is the same as the intervals $t_0$, $A_1$. The equivalent circuits are as shown in Figs. 5a–c sequentially.

After analysing the operation waveform, ZVS can be achieved on the secondary side when turning on but the soft-switching is lost on the primary side. The time of the zero current is derived from

\[ t_0 = \frac{-6\phi - 4\pi - 6DM + 4\pi M}{3(M + 1)} \]  \hspace{1cm} (5)

**3.1.3 Mode A3:** If $0 \leq \phi < D$ and $t_0 = 0$, the operation waveforms are shown in Fig. 4.43. Since $\phi < D$ the effective value of the phase shift is negative in Modes A1–A3. That is why phase shift drift happens.

During the time interval $t_0$, the analysis is almost the same as the interval $t_0$, $A_2$ except that the current $i_A$ ends up to a positive value instead of 0. Another difference is that when $Q_1$ is turned ON during the interval $t_0$ to $t_1$, the current will go through the MOSFET other than its body diode.

At $t_0$, $Q_1$ is turned OFF as shown in Fig. 5g. However, the current $i_S$ forces the body diode of $Q_6$ to conduct. The voltage across $L_A$ will be $(nV_i - V_o)/3n$ which cause $i_A$ to decrease to a negative value at $t_1$.

**3.1.4 Mode A4:** As shown in Fig. 4.44, the Mode A5 conditions are $\phi > D$, $i(S_{off}) < 0$ and $i(S_{on}) < 0$.

At $t_0$, $S_1$ is turned ON. Therefore, $S_1$, $S_2$ and $S_3$ are conducting on the primary side and $Q_3$, $Q_4$ and $Q_5$ are turned ON as shown in Fig. 5j. The voltage across $L_A$ is $(nV_i - V_o)/3n$ which will induce $i_A$ to increase.

At $t_0$, $Q_4$ is turned OFF. $i_C$ will keep the positive direction thus the body diode of $Q_1$ is conducting. The equivalent circuit for the interval $t_0$, $A_3$ is shown in Fig. 5k. Just before $t_0$, the switch $S_3$ is turned OFF while its body diode will be conducting.

**3.1.5 Mode A5:** The constraint conditions are $\phi > D$, $i(S_{off}) < 0$ and $i(S_{on}) < 0$. But this mode can be further divided into three different cases as shown in Figs. 4.5a–4.5c where $I_{in}$ represents the time interval when negative current conducting from the time $S_1$ turned OFF to the time $S_3$ turned OFF.

**Case a:** When $\phi \geq \pi/3$ and $t_0 < D - \phi + \pi/3$, the operation waveforms are shown in Fig. 4.5a. At $t_0$, $S_1$ is turned ON. $S_1$, $S_3$ and $S_2$ are conducting on the primary side as shown in Fig. 5n. On the secondary side, $Q_3$ and $Q_4$ are turned ON and the body diode of $Q_3$ is conducting. The voltage across $L_A$ is $(nV_i - V_o)/3n$ which will cause $i_A$ to increase in the positive direction.

For the time interval between $t_0$ and $t_2$, two actions happening. First, $S_3$ is turned OFF when the body diode of $S_6$ is conducting resulted from the direction of the current $i_S$, as shown in Fig. 5l. Then, since $Q_3$ is turned ON, the MOSFET is conducting instead of...
its body diode. The voltage across $L_A$ is $(2V_i + V_o)/3n$ which will cause $i_A$ to increase in the positive direction.

For the interval $t_2$ to $t_3$, the equivalent circuit is shown in Fig. 5j. The body diode of $Q_1$ is conducting after $Q_4$ is turned OFF at the time $t_2$ due to the positive direction of $i_a$. 

Fig. 5 Equivalent circuits of the three-phase DAB converter for the dead-time effect analysis
At \( t_3 \), the polarity of the current \( i_C \) changes from positive to negative. Hence, the body diode of \( S_3 \) is conducting as shown in Fig. 5k.

The time of the negative current in the waveform as shown in Fig. 4.45a is derived as

\[
t_{iN} = \frac{3D - 2\pi + 3DM + 2\pi M - 3M\phi}{3M}
\]  

(6)

Case b: When \( \phi \geq \pi/3 \) and \( t_{iN} > D - \phi + \pi/3 \), the operation waveforms are shown in Fig. 4.45b. During the interval \( t_5 \) to \( t_6 \), this interval can be analyzed with the same procedure like an interval \( t_5 \sim t_6 \) in Case a of Mode A5. The equivalent circuit is illustrated in Fig. 5n.

At \( t_6 \), \( S_3 \) is turned OFF as shown in Fig. 5o. However, the body diode of \( S_6 \) is forced to conduct due to the positive \( i_C \). The voltage across \( L_A \) is \( (2V_i + V_o)/3n \) which will cause \( i_A \) to increase in the positive direction.

At \( t_7 \), the polarity of the current \( i_C \) changes from negative to positive. Although \( S_3 \) is not turned ON, its body diode is conducting as shown in Fig. 5p.

The time of the negative current in the waveform as shown in Fig. 4.45b is derived from

\[
t_{iN} = \frac{3D - 2\pi + 6DM + 3\pi M - 6M\phi}{6M}
\]  

(7)

Case c: When \( 0 \leq \phi < \pi/3 \) the operation waveforms are shown in Fig. 4.45c. At \( t_8 \), \( S_1 \) is turned ON, \( S_1, S_2 \) and \( S_6 \) are conducting on the primary side as shown in Fig. 5h. On the secondary side, \( Q_3, Q_4 \) and \( Q_5 \) are turned ON. The voltage across \( L_A \) is \( (nV_i - V_o)/3n \) which will cause \( i_A \) to increase in the positive direction.

At \( t_9 \), \( Q_4 \) is turned OFF while the body diode of \( Q_1 \) is conducting due to the positive \( i_A \) as shown in Fig. 5q.

From the time interval \( t_5 \) to \( t_6 \), the equivalent circuit is shown in Fig. 5j. At \( t_6 \), \( S_1 \) is turned OFF then the body diode of \( S_6 \) is conducting as shown in Fig. 5j.

At \( t_7 \), the direction of the current \( i_C \) changes so the body diode of \( S_1 \) conducts. Then, \( Q_1 \) is turned ON as shown in Fig. 5r.

The time of the negative current in the waveform as shown in Fig. 4.45c is derived as

\[
t_{iN} = \frac{3D - 2\pi + 3DM + 2\pi M - 3M\phi}{3M}
\]  

(8)

<table>
<thead>
<tr>
<th>Table 2</th>
<th>Transmission power and constrain conditions for the boost state</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mode A1</td>
<td>[ \frac{2\pi(M - 1)}{3M} \leq D \leq \frac{\pi}{3} \quad \text{and} \quad 0 \leq \phi &lt; \frac{4\pi + 6DM - 4\pi M}{3(M + 1)} ]</td>
</tr>
<tr>
<td>Mode A2</td>
<td>[ \frac{2\pi(M - 1)}{3M} \leq D \leq \frac{\pi}{3} \quad \text{and} \quad \frac{4\pi + 6DM - 4\pi M}{3(M + 1)} \leq \phi &lt; \frac{3D - 2\pi + 2\pi M}{3} ]</td>
</tr>
<tr>
<td>Mode A3</td>
<td>[ \begin{cases} 0 \leq D \leq \frac{2\pi(M - 1)}{3M} \quad \text{and} \quad 0 \leq \phi &lt; \frac{3DM - 2\pi M + 2\pi}{3} \ 0 \leq D \leq \frac{\pi}{3} \quad \text{and} \quad \frac{3DM - 2\pi M + 2\pi}{3} \leq \phi &lt; D \end{cases} ]</td>
</tr>
<tr>
<td>Mode A4</td>
<td>[ \begin{cases} 0 \leq D \leq \frac{\pi}{3} \quad \text{and} \quad \frac{3D - 2\pi + 2\pi M}{3} \leq \phi &lt; \frac{3D - 2\pi + 3\pi M}{6} \ \frac{2\pi(M - 1)}{3M} \leq D \leq \frac{\pi}{3} \quad \text{and} \quad \frac{3D - 2\pi + 2\pi M}{3} \leq \phi &lt; \frac{3D - 2\pi + 3\pi M}{6} \end{cases} ]</td>
</tr>
<tr>
<td>Mode A6a</td>
<td>[ \begin{cases} 0 \leq D \leq \frac{2\pi(M - 1)}{3M + 1} \quad \text{and} \quad \frac{3D + 3DM - 2\pi + 2\pi M}{3} \leq \phi &lt; \frac{\pi}{3} \ 0 \leq D \leq \frac{\pi}{3} \quad \text{and} \quad \frac{\pi}{3} \leq \phi &lt; \frac{2\pi}{3} \ \frac{\pi}{3} \leq \phi &lt; \frac{2\pi}{3} \end{cases} ]</td>
</tr>
<tr>
<td>Mode A6b</td>
<td>[ \begin{cases} 0 \leq D \leq \frac{\pi}{3} \quad \text{and} \quad \frac{2\pi(M - 1)}{3(M + 1)} \leq \phi &lt; \frac{\pi}{3} \ \frac{2\pi(M - 1)}{3(M + 1)} \leq D \leq \frac{\pi}{3} \quad \text{and} \quad \frac{3D + 3DM - 2\pi + 2\pi M}{3} \leq \phi &lt; \frac{2\pi}{3} \ \frac{3D - 2\pi + 2\pi M}{3} \leq \phi &lt; \frac{2\pi}{3} \end{cases} ]</td>
</tr>
<tr>
<td>Mode A5a</td>
<td>[ \begin{cases} \frac{\pi}{3} \leq D \leq \frac{\pi}{3} \quad \text{and} \quad \frac{\pi}{3} \leq \phi &lt; \frac{3D + 3DM - 2\pi + 2\pi M}{3M} \ \frac{\pi}{3} \leq D \leq \frac{\pi}{3} \quad \text{and} \quad \frac{3D - 2\pi + 3\pi M}{6M} \leq \phi &lt; \frac{3D + 6DM - 2\pi + 3\pi M}{6M} \ \frac{\pi}{3} \leq D \leq \frac{\pi}{3} \quad \text{and} \quad \frac{3D - 2\pi + 2\pi M}{3M} \leq \phi &lt; \frac{\pi}{3} \end{cases} ]</td>
</tr>
<tr>
<td>Mode A5b</td>
<td>[ \begin{cases} \frac{\pi}{3} \leq D \leq \frac{\pi}{3} \quad \text{and} \quad \frac{\pi}{3} \leq \phi &lt; \frac{3D + 3DM - 2\pi + 2\pi M}{3M} \ \frac{\pi}{3} \leq D \leq \frac{\pi}{3} \quad \text{and} \quad \frac{3D - 2\pi + 3\pi M}{6M} \leq \phi &lt; \frac{3D + 6DM - 2\pi + 3\pi M}{6M} \ \frac{\pi}{3} \leq D \leq \frac{\pi}{3} \quad \text{and} \quad \frac{3D - 2\pi + 2\pi M}{3M} \leq \phi &lt; \frac{\pi}{3} \end{cases} ]</td>
</tr>
<tr>
<td>Mode A5c</td>
<td>[ \begin{cases} \frac{\pi}{3} \leq D \leq \frac{\pi}{3} \quad \text{and} \quad \frac{\pi}{3} \leq \phi &lt; \frac{3D + 3DM - 2\pi + 2\pi M}{3M} \ \frac{\pi}{3} \leq D \leq \frac{\pi}{3} \quad \text{and} \quad \frac{3D - 2\pi + 3\pi M}{6M} \leq \phi &lt; \frac{3D + 6DM - 2\pi + 3\pi M}{6M} \ \frac{\pi}{3} \leq D \leq \frac{\pi}{3} \quad \text{and} \quad \frac{3D - 2\pi + 2\pi M}{3M} \leq \phi &lt; \frac{\pi}{3} \end{cases} ]</td>
</tr>
</tbody>
</table>
To summarise the soft-switching condition in Mode A5, ZVS can be achieved on the secondary side when turning on but the soft-switching is lost on the primary side.

### 3.1.6 Mode A6: The operational waveforms of Mode A6 are shown in Figs. 4.6(a) and 6(b). The constraint conditions of Mode A6 are \( \phi > D, i(S_{oA}) > 0 \) and \( i(S_{oA}) > 0 \). In this mode, the dead time does not affect the waveforms and this mode is similar to the normal operation mode of the three-phase DAB converter. This mode can be further divided into two cases.

- **Case a**: The constraint condition of this case is \( 0 \leq \phi < \pi/3 \) and its waveforms are shown in Fig. 4.6(a). At \( t_0 \), \( S_4 \) is turned OFF. Since the current \( i_A \) is negative, the body diode of \( S_1 \) is conducting. Besides, \( S_3 \) and \( S_2 \) are conducting on the primary side as shown in Fig. 5x. On the other hand, \( Q_3, Q_4 \) and \( Q_5 \) are turned ON. The voltage across \( L_q \) is \( (nV_i - V_o)/3n \) which will cause \( i_A \) to increase in the positive direction. The zero crossing of the current is later than the moment when \( S_1 \) is turned ON. Therefore, ZVS is achieved. At \( t_0 \), \( Q_4 \) is turned OFF. Due to the positive \( i_o \), the body diode of \( Q_0 \) is conducting as shown in Fig. 5y.

- **Case b**: The constraint condition of this case is \( \pi/3 < \phi \leq 2\pi/3 \) and its waveforms are shown in Fig. 4.6(b). At \( t_0 \), \( S_4 \) is turned OFF. Since the current \( i_A \) is negative, the body diode of \( S_1 \) is conducting as shown in Fig. 5m. During the interval \( t_0 \) to \( t_1 \), \( S_1 \) is turned ON and ZVS is achieved.

At \( t_1 \), \( Q_3 \) is turned OFF. Since the current \( i_B \) is negative, the body diode of \( Q_2 \) is conducting as shown in Fig. 5n.

### 3.2 Buck state (M < 1)

#### 3.2.1 Mode B1: When \( 0 \leq \phi < D, I_o > 0 \) and \( t_0 = D - \phi \), the operation waveforms of the Mode B1 is shown in Fig. 6B1.

At \( t_0 \), \( S_1 \) is turned ON. Although \( Q_1 \) is not turned ON, its body diode is conducting due to the positive \( i_A \) as shown in Fig. 5q. The voltage across \( L_A \) is \( (nV_i - V_o)/3n \). Since \( M < 1 \) in the buck state, it will cause \( i_A \) to increase in the positive direction.

At \( t_0 \), \( S_3 \) is turned OFF as shown in Fig. 5u. However, the body diode of \( S_2 \) is conducting depending on the polarity of the current \( i_L \). If we focus on Phase C, the voltage across \( L_C \) is \( - (nV_i - V_o)/3n \) which will cause \( i_C \) to decrease in the positive direction. At \( t_0 \), \( i_L \) ends.

For the time interval \( t_1 \) to \( t_3 \), the equivalent circuit is shown in Fig. 5v. The analysis for the time interval \( t_1 \sim t_3 \) is very similar to the analysis for the time interval \( t_1 \sim t_3 \) as shown in Fig. 5d. The difference is that the polarity of \( i_A \) and \( i_B \) is opposite. The time duration of the zero current is calculated as

\[
t_0 = \frac{2(3D - 2\pi + 2\pi M)}{3(M + 1)}
\]

The constraint conditions and transmission power expression are shown in Table 3. After analysing the operation waveform, the ZVS can be achieved in the switches of the primary side during turning on at the same time the ZCS can be achieved in the switches of the secondary side during turning on and off. This mode may be utilised to increase the efficiency when the ZVS is lost in the light load condition of the regular modulation.

#### 3.2.2 Mode B2: When \( 0 \leq \phi < D, I_o > 0 \) and \( t_0 > D - \phi \), the waveforms are shown in Fig. 6B2.

The analysis for the time interval \( t_0 \sim t_1 \) is the same as the time interval \( t_0 \sim t_1 \) in Mode B1.

Although the current \( i_C \) is zero same as in the previous analysis at \( t_0 \), \( Q_3 \) is turned ON as shown in Fig. 5x. The voltage relationship can be derived based on the analysis for the time interval \( t_0 \sim t_1 \) in Mode A1. The voltages are derived from

\[
\begin{align*}
V_{AO} &= \frac{3(V_i - nV_o)}{6} \\
V_{BO} &= nV_o/3 \\
V_{CO} &= \frac{3(V_i + nV_o)}{6} \quad (10) \\
V_{HA} &= 0
\end{align*}
\]

At \( t_0 \), the current \( i_C \) is zero and \( Q_3 \) is still turned OFF as shown in Fig. 5x. The analysis is very similar to the analysis of the time interval \( t_1 \sim t_3 \) as shown in Fig. 5d. The difference is that the polarity of \( i_A \) and \( i_B \) is opposite. The time duration of zero current is derived in (11). Same as Mode B1, the ZVS can be achieved on the primary side when turning on while ZCS can be achieved on the secondary side when turning on and off. This mode can be utilised to increase the efficiency when the ZVS is lost in the light load condition of the regular modulation

\[
t_0 = \frac{2(3D - 2\pi + 2\pi M)}{3(M + 1)}
\]

#### 3.2.3 Mode B3: When \( \phi > D \) and \( t_0 > 0 \), the operation waveforms are shown in Figs. 6B3a and 6B3b. However, this mode can be divided further into two cases and will be discussed below:
Case a: The constraint condition of this case in Mode B3 is $D \leq \varphi < \pi/3$ and its operation waveforms are shown in Fig. 6B3a.

The analysis for the time interval $t_0 - t_i$ can be done referred to the time interval $t_0 - t_i$ in Case c of Mode A5. The equivalent circuits are shown in Figs. 5h, q and j.

At $t_i$, $i_c$ is zero according to aforementioned analysis. $Q_3$ is still open as shown in Fig. 5j. This case is very similar to the time interval $t_0 - t_i$, in Mode A1. The voltage equations are found in (10). The time duration of zero current is calculated as:

$$t_0 = \frac{2(3D - 2\pi + 3DM + 2eM - 3M\varphi)}{3(M + 1)}$$  \hspace{1cm} \text{(12)}

Case b: The constraint condition of this case in Mode B3 is $\varphi \geq \pi/3$ and its operation waveforms are shown in Fig. 6B3b.

The analysis for the time interval $t_0 - t_i$ can be done referred to the time interval $t_0 - t_i$ in Case a of Mode A5. The equivalent circuits are Figs. 5n, i and j.

The analysis for the time interval $t_0 - t_c$, is similar to the time interval $t_0 - t_i$, in Case c of Mode B3. The time duration of zero current is derived as (13). To summarise the soft-switching condition, the ZVS can be achieved on both primary side and secondary side:

$$t_0 = \frac{2(3D - 2\pi + 3DM + 2eM - 3M\varphi)}{3(M + 1)}$$  \hspace{1cm} \text{(13)}

3.2.4 Mode B4: When the time $t_0$ is zero as shown in Fig. 6B4a and B4b, it can be observed that this mode is the normal operation mode for the three-phase DAB converter in the buck state. It can be divided into two cases by $0 \leq \varphi < \pi/3$ and $\pi/3 \leq \varphi < 2\pi/3$. The analysis of this mode is the same as Mode A6 for the boost state.

3.3 Matching state ($M = 1$)

3.3.1 Mode C1: When $0 \leq t_0 < D$ the operation waveforms are shown in Figs. 7C1a and C1b. However, this mode can be divided further into two cases and will be discussed below:

Case a: When $0 \leq \varphi < \pi/3$ the waveforms of this case are shown in Fig. 7C1a. The analysis for the time interval $t_0 - t_i$ is the same as the time interval $t_0 - t_i$ in Mode A4 in the boost state as shown in Fig. 5i. The analysis for the time interval $t_0 - t_i$ is similar to the time interval $t_0 - t_i$ in Mode B1 in the buck state as shown in Figs. 5g and u. However, for the interval $t_0$ to $t_i$, the voltage across $L_A$ is $(nV_C - V_o)/3n$, which is zero considering the matching state ($M = 1$). Therefore, the current $i_a$ remains the same instead of increasing linearly in Mode B1.

The analysis for the time interval $t_0 - t_i$ is the same as the time interval $t_0 - t_i$ in Case c of Mode A5 in the boost state as shown in Fig. 5r. The time duration of zero current is derived as (14). The constraint conditions and transmission power are shown in Table 4

$$t_0 = \frac{D - 2p + DM + M\varphi}{2M - 1}$$  \hspace{1cm} \text{(14)}

Case b: When $\varphi \geq \pi/3$ the waveforms of this case can be found in Fig. 7C1b. The analysis for the time interval $t_0 - t_i$ is the same as the time interval $t_0 - t_i$ in Case b in Mode B3 of the buck state as shown in Figs. 5n, i and j.

During the time interval $t_0 - t_i$, the equivalent circuit is shown in Fig. 5k. The voltage across $L_A$ is zero so the current $i_a$ stay as the same. The time duration of zero current is derived as (15). The ZVS can be achieved on both the primary side and secondary side

$$t_0 = \frac{6D + 3\varphi - 5e + 6DM + 5M\varphi - 9MQ}{12M - 6}$$  \hspace{1cm} \text{(15)}

3.3.2 Mode C2: The waveforms of this mode are shown in Fig. 7C2. Roughly speaking, the constraint condition is $t_0 = T$, which means the current is zero all the time. However, the current is not always zero but very close to zero. After the switching, the current not increases or decreases like the other modes but stay the same value due to the matching of the voltage. At $t_0$, $S_1$ is turned ON and its equivalent circuit is shown in Fig. 5r. Since the voltage across the leakage inductance is zero, the current is a very small value. The current is small but needs to force the body diode to conduct like $S_3$ as shown in Fig. 5r.

For the time interval $t_0 - t_i$, the equivalent circuit is shown in Fig. 5v. Since there is almost no current in the leakage inductor and all switches for Phase C are closed, $V_{CO}$ and $V_{CO'}$ are zero. The voltages $V_{HC}$ and $V_{HC'}$ are derived to be $V_o/2$ and $V_o/2$. Based on

Table 3: Transmission power and constrain conditions for the buck state

<table>
<thead>
<tr>
<th>Mode</th>
<th>Constraint conditions</th>
<th>Transmission Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>B1</td>
<td>$\frac{2\pi(1-M)}{3} \leq D &lt; \pi/3$ and $0 \leq \varphi &lt; (M - 1)(3D - 4\pi) / (3(M + 1))$</td>
<td>$P = -\mu V_i^2 (M - 1)(3D - 4\pi)^2 / 18L_{eo}(M + 1)$</td>
</tr>
<tr>
<td>B2</td>
<td>$\frac{2\pi(1-M)}{3} \leq D &lt; \pi/3$ and $0 \leq (M - 1)(3D - 4\pi) / (3(M + 1)) &lt; \varphi &lt; M$</td>
<td>$P = -\mu V_i^2 / (\pi - 2\pi)$</td>
</tr>
<tr>
<td>B4a</td>
<td>$0 \leq D &lt; \frac{2\pi(1-M)}{3} &lt; \frac{2\pi}{3}$</td>
<td>$P = \mu V_i^2 / (\pi - \varphi)$</td>
</tr>
<tr>
<td>B4b</td>
<td>$0 \leq D &lt; \frac{2\pi}{3}$</td>
<td>$P = \mu V_i^2 / (\pi - \varphi)$</td>
</tr>
<tr>
<td>B3a</td>
<td>$\frac{2\pi(1-M)}{3} \leq D &lt; \pi/3$</td>
<td>$D \leq \varphi &lt; (3D - 2\pi + 2\pi M) / (3M)$</td>
</tr>
<tr>
<td></td>
<td>$\frac{\pi(2-M)}{3(M + 1)} \leq D &lt; \frac{\pi}{3}$</td>
<td>$0 \leq \varphi &lt; (3D - 2\pi + 2\pi M) / (3M)$</td>
</tr>
<tr>
<td></td>
<td>Power $P = \mu V_i^2 (3\varphi - 4\pi) / 18L_{eo}(M + 1)$</td>
<td></td>
</tr>
<tr>
<td>B3b</td>
<td>$\frac{\pi(2-M)}{3(M + 1)} \leq D &lt; \frac{\pi}{3}$</td>
<td>$\varphi &lt; \frac{3D - 2\pi + 2\pi M}{3M}$</td>
</tr>
<tr>
<td></td>
<td>Power $P = \mu V_i^2 (6\varphi - 17\pi\varphi + 36\pi^2 + 15\pi^2 - 18\pi^2 - 24\pi D + 18D\varphi - 24\pi D M + 18D M^2 + 54\pi M\varphi) / 18L_{eo}(M + 1)$</td>
<td></td>
</tr>
</tbody>
</table>
vAO and vAO′ are Vi/2 and Vo/2, respectively. The current is still a very small value.

The current almost zero because of the matching of the voltage across the leakage inductance. However, very small current still exists in the circuit. For the time interval t0 to t1, the circuit is shown in Fig. 5r. From time interval t1 to t2, the circuit is shown in Fig. 5v. Based on the analysis, the constraint condition is 0 ≤ ϕ < D. The power is close to zero, P≈0.

### 3.3.3 Mode C3

When the time t0 is zero as shown in Fig. 7C3a and C3b, it can be observed that this mode is the normal operation mode for the three-phase DAB converter. It can be divided into two cases by $D \leq \phi < \frac{\pi}{3}$ and $\frac{\pi}{3} \leq \phi < 2\frac{\pi}{3}$.

#### Table 4a

<table>
<thead>
<tr>
<th>Mode C1a</th>
<th>Constraint</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 ≤ D &lt; $\frac{\pi}{6}$</td>
<td>$\phi &lt; 2D$</td>
<td>$P = \frac{-MV^2i(21\phi - 9D + 2\pi + 9DM^2 + 3M^2\phi + 4nM - 30M\phi)}{6L_0\omega\pi(2M - 1)}$</td>
</tr>
<tr>
<td>$\frac{\pi}{6} \leq D &lt; \frac{\pi}{3}$</td>
<td>$\phi &lt; \frac{\pi}{2}$</td>
<td>$P = \frac{-MV^2i(108D^2M^2 - 108D^2 - 252DM^2\phi + 84\pi DM^2 + 180DM\phi - 132\pi DM + 144\pi D)}{72L_0\pi(2M - 1)}$</td>
</tr>
</tbody>
</table>

#### Table 4b

<table>
<thead>
<tr>
<th>Mode C2</th>
<th>Constraint condition</th>
<th>Transmission power</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 ≤ ϕ &lt; D</td>
<td></td>
<td>$P = 0$</td>
</tr>
</tbody>
</table>

#### Table 5

| Experiment specifications | Input DC voltage $V_i$ (boost/buck/matching) 26 V/34 V/30 V | output DC voltage $V_o$ 180 V | switching frequency $f$ 50 kHz | leakage inductance $L$ 1.76 μH | transformer ratio $n$ 1:6 | input capacitor $C_1$ 100 μF | output capacitor $C_2$ 40 μF |

### 4 Experiment verification

To verify the dead-time effect analysis, a three-phase DAB converter experiment setup is built.

Three individual transformers with 1:6 turn ratio are utilised. For this boost stage, the input voltage is 26 V, and the output voltage is 180 V. As for the buck state, the input and output voltage are set as 34 and 180 V, respectively. For the matching state, the input is 30 V and the output voltage is 180 V. The detailed specifications of the experiment are shown in Table 5. The experimental results for the boost state, the buck state and the matching state are shown in Fig. 8. It can be found that the experiment results match the simulation results in Figs. 4, 6 and 7.

The experiments are also conducted to verify the analytical transmission power equations. The transmission power comparison...
is shown in Fig. 9. The benchmark is the simulated transmission power of the conventional operation which is the dashed line shown in Fig. 9. The dead time of the dashed line is a relatively smaller value \( D \approx 0 \) than the dead-time effect analysis to ensure the conventional operation. The so-called phase shift drift exists in all the three states. Generally speaking, the dead time decreases the transmission power of the three-phase DAB converter. It can be found there is a sudden rise at \( \pi/3 \) in the conventional operation.

**Fig. 8** Experiment results (Time scale: 15 μs/div). The experiment conditions are summarized as following. Boost state:
(a) \( D = 0.96, \phi = 0 \); (b) \( D = 0.70, \phi = 0.48 \); (c) \( D = 0.52, \phi = 0.48 \); (d) \( D = 0.35, \phi = 0.52 \); (e) \( D = 0.55, \phi = 1.07 \); (f) \( D = 0.96, \phi = 1.29 \); (g) Mode A1: \( D = 0.52, \phi = 0.87 \); (h) \( D = 0.35, \phi = 0.99 \); (i) \( D = 0.38, \phi = 1.11 \).

Buck State:
(j) \( D = 0.44, \phi = 0.14 \); (k) \( D = 0.40, \phi = 0.52 \); (l) \( D = 0.58, \phi = 0.82 \); (m) \( D = 0.96, \phi = 1.17 \); (n) \( D = 0.38, \phi = 0.62 \); (o) \( D = 0.57, \phi = 1.08 \).

Matching state:
(p) \( D = 0.85, \phi = 0.98 \); (q) \( D = 0.70, \phi = 1.12 \); (r) \( D = 0.91, \phi = 0.47 \); (s) \( D = 0.38, \phi = 0.77 \); (t) \( D = 0.38, \phi = 1.11 \).
due to the operation modes change of the three-phase DAB converter from the operation with the phase shift in \( 0 \leq \phi < \pi/3 \) and the operation with the phase shift in \( \pi/3 \leq \phi < 2\pi/3 \).

### 5 Conclusion

In this paper, the dead-time effect of the three-phase DAB converter is comprehensively analysed. The detailed operation states, transmission power, constrain equations and switching characteristic are provided. The dead-time phenomena in single-phase DAB converter, such as voltage polarity reversal, voltage sag and phase shift, is also exist in the three-phase topology. The experiment results and simulation results verified the theoretical analysis. This study can help to better design of the three-phase DAB converter to avoid the dead-time effect and better understanding of the operation with dead-time effect. The future work can also focus on how to utilise the dead-time effect to reduce the power loss at light load condition.

### 6 References


