DC-Bus Design with Hybrid Capacitor Bank in Single-Phase PV Inverters

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***Abstract*— The active or passive decoupling method has to be utilized to deal with the second-order harmonic existing in the DC-bus of the grid-tied single-phase inverters. Compared with the active decoupling method, the passive decoupling method is simpler, cheaper and more reliable. The electrolytic capacitors are usually used in the DC-bus as typical passive decoupling components. The film capacitors can be added in parallel with the electrolytic capacitor to help filtering out the high frequency harmonics to extend the electrolytic capacitors' life. In addition, the LC resonant filter can be utilized for the decoupling purpose to achieve better performance. However due to the relatively low resonant frequency, it results in large inductance which will significantly increase the size and cost of the system. A current sharing method is proposed in this paper. With this method, an inductor with reasonable size can be utilized in the LC resonant filter to further extend the electrolytic capacitors' life. In this paper, the design procedure of the hybrid capacitor bank for the single-phase inverter with unipolar modulation will be discussed. The simulation and experimental results will be provided to verify the design of the hybrid capacitor bank for a 3kW single-phase PV inverter.**

***Keywords*— DC-bus capacitor bank; grid-tied single-phase inverter; passive decoupling.**

I. INTRODUCTION

Most experts believe the renewable energy share of the global energy supply will be at least doubled to 40% even 60% by the year of 2050 [1]. Among them, the solar energy is very promising because its market grows significantly since 2010. Therefore, the grid-tied PV inverter has been a hotspot in research these years.

The single-phase grid-tied inverter with 240 VAC output for residential applications is very popular in the market [2]. The stable DC-bus should be achieved for the interface between the MPPT DC/DC converter and single-phase inverter in the two-stage PV inverter. Moreover, the stable DC-bus is desired for future integration with energy storage unit. However, the single-phase inverter suffers from the double grid frequency harmonic on the DC-bus. Power decoupling techniques are studied to deal with this problem [3], [4]. A buck-type active filter is proposed to absorb the second-order current ripple as an active power decoupling method in [5]. An integrated dual-active-bridge converter based active filter is proposed to filter the second order harmonic from on board battery charger [6]. However, the active components will increase the complexity of the whole system. Considering additional switches and their gate drivers, current sensors and inductors, the active power decoupling methods may not significantly reduce the space and size compared to the passive method. Thus, the passive power decoupling method is widely used in the commercial products because of simple structure and reliability. Capacitors are usually applied as the energy buffer with passive power decoupling method. In [7], the minimum energy and capacitance requirements for the DC-bus capacitor are discussed. Besides, the double frequency harmonic, the high frequency harmonics still exist in the DC-bus. The high frequency harmonics caused by the PWM of the single-phase inverter needs to be considered when designing the DC-bus. Unipolar SPWM of the single-phase inverter is widely utilized in grid-tied PV application because the dominating switching harmonic frequency with unipolar modulation is twice of the switching frequency. Thus the size of the output filter and DC-bus capacitors will be reduced a lot compared to those with bipolar SPWM.

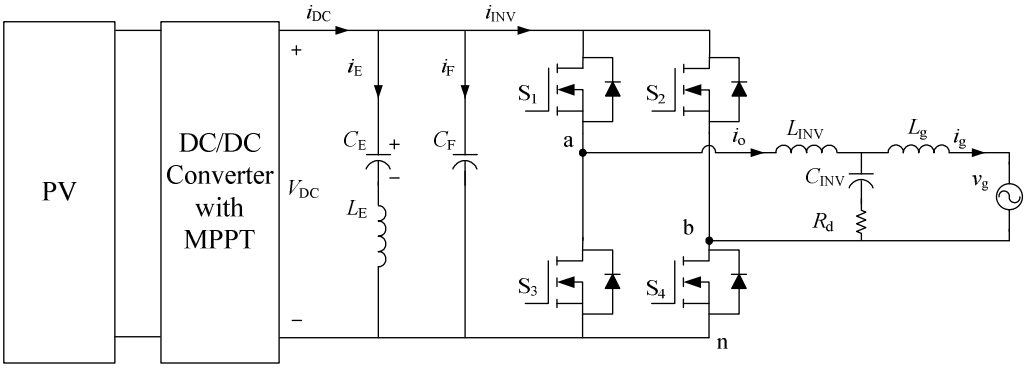

Fig. 1 Grid-tied single-phase PV inverter with a hybrid capacitor bank.

The capacitors used in DC-bus are discussed in [8]. Generally, Aluminum Electrolytic Capacitors is superior in the energy density and capacitance, which makes it suitable for the energy buffer purpose. The Metallized Polypropylene Film Capacitors is superior in terms of ripple current and frequency, which makes it suitable for the high frequency harmonics filtering purpose. The electrolytic capacitors are usually used as the energy buffer for the power decoupling purpose. However, the life time of the electrolytic capacitor is limited by the RMS value of the ripple current. Thus, the electrolytic capacitor is usually oversized considering additional high frequency harmonics caused by PWM. Thus, it is feasible to design a DC-bus capacitor bank to combine the advantages of both electrolytic capacitor and film capacitor. Based on this idea, the electrolytic capacitor will be designed for the double frequency harmonic while the film capacitor will be designed to filtering out the high frequency harmonics. In addition, the resonant LC filter in DC-bus is employed in single-phase active rectifiers [9] to avoid oversizing of the DC-bus capacitor and to obtain less voltage variation on the DC-bus. However, since the resonant frequency for LC filter is low, the weight and size of the additional inductor are considerable. Besides, the voltage across the capacitor of the LC branch may be higher than the maximum DC-bus voltage. In this paper, a current sharing method is proposed that a reasonably small inductor is added in series with the electrolytic capacitor to form an LC resonant filter to further extend the life time of the electrolytic capacitor. At the same time, the size and cost of the system won't be sacrificed too much.

In this paper, a hybrid capacitor bank, including film capacitors and the LC resonant filter with small inductor is proposed for the single-phase grid-tied PV inverter as shown in Fig. 1. C_E is the electrolytic capacitor bank and, L_E is the inductor with reduced size, thus L_EC_E represents the LC resonant filter. C_F represents the film capacitor. The detailed design procedure of the electrolytic and film capacitors is discussed in section II. The LC resonant filter design for this application is discussed in section III. Simulation and experimental results are provided to verify the proposed hybrid capacitor bank in section IV.

II. Design of the Hybrid Capacitor Bank

A. Design of the electrolytic capacitor

A system of single-phase inverter for solar energy smart home applications is shown as Fig. 1. The hybrid capacitor bank is expected to filtering out the harmonics caused by the single-phase inverter to achieve a stable DC-bus voltage. The electrolytic capacitor is used to buffer the double frequency harmonic while the film capacitor is responsible for the high frequency harmonics. It is assumed that the grid voltage is $v_g(t) = V_g \cos(\omega t)$ and the output current is $i_g(t) = I_g \cos(\omega t + \phi)$, where ϕ is the phase angle with respect to the grid voltage. For simplicity, harmonics in the output current of the inverter i_o are not considered at this time, which won't cause much error [10]. Therefore, it is assumed that $i_o(t) \approx i_g(t) = I_g \cos(\omega t + \phi)$. With the unit power factor, the capacitance is designed by small signal analysis in [7].

$$C_E = \frac{P_o}{2\pi f V_{DC} \Delta V} = \frac{V_g I_g}{2\pi f V_{DC} \Delta V} \tag{1}$$

where f represents the grid frequency which is 60Hz in North America. P_o is chosen as 3kW and V_{DC} is the 400V for our case. ΔV is the maximum allowed voltage variation in DC-bus and is chosen as 5%. The RMS current going through the electrolytic capacitor is obtained as following.

$$i_{C_E,\mathrm{RMS}} = \frac{P_o}{\sqrt{2} V_{DC}} \tag{2}$$

B. Design of the film capacitor

The unipolar SPWM modulation is applied for the single-phase inverter because the switching harmonic frequency of the inverter output is twice of its switching frequency. Therefore, the size of passive component in the system will be reduced. The RMS current of the three phase inverter and bipolar SPWM single-phase inverter are calculated in [10]. However, the RMS current analysis of the unipolar SPWM single-phase inverter is not discussed. The unipolar SPWM modulation process is illustrated in Fig. 2. It is assumed that the inverter's voltage is in the same phase as the grid voltage.

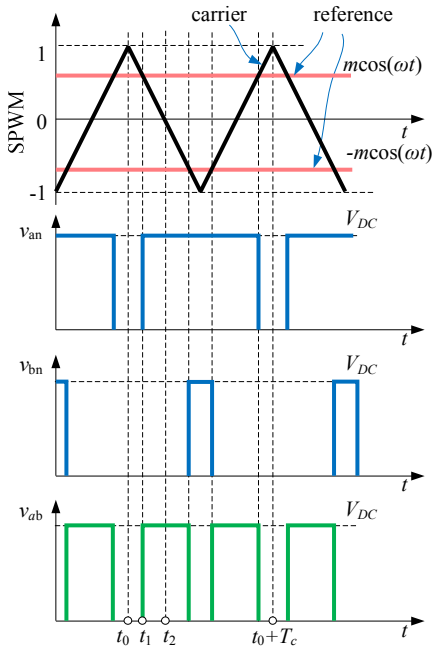

Fig. 2 Unipolar SPWM modulation illustration.

In Fig. 2, the two red lines represent the two reference signals for unipolar modulation. The voltage across S_3 and S_4 are shown as blue curves and the green curve represents the inverter's output voltage. ω represents the radial speed of the grid, m is the modulation index and T_c represents the period of the carrier signal. Based on the basic geometric principles,

$$\frac{m\cos(\omega t_0)}{1} = \frac{t_2 - t_1}{t_2 - t_0} = \frac{t_2 - t_1}{T_c / 4} \qquad 0 \le \omega t_0 \le \pi / 2 \tag{3}$$

$$t_1 - t_0 = \frac{T_c}{4} - \frac{T_c}{4} m\cos(\omega t) \tag{4}$$

So the duty cycle for S_3 is

$$d_{an}(t) = \frac{T_c - 2\times(t_1 - t_0)}{T_c} = \frac{1}{2}(1 + m\cos(\omega t)) \tag{5}$$

Based on the same procedure, the duty cycle for S_4 is

$$d_{bn}(t) = \frac{1}{2}(1 + m\cos(\omega t + \pi)) \tag{6}$$

Thus the duty cycle for unipolar SPWM modulation can be expressed as (7).

$$d_{ab}(t) = d_{an}(t) - d_{bn}(t) = \left|m\cos(\omega t)\right| \tag{7}$$

The squared input current of the single-phase inverter can be expressed by the product of its squared output current and the duty cycle of the unipolar SPWM modulation. The square of the input current can be calculated by (8).

$$i_{INV}^2(t) = d_{ab}(t)\cdot i_o^2(t) = \left|m\cos(\omega t)\right|\cdot I_g^2\cos^2(\omega t + \phi) \tag{8}$$

The RMS value of the input current can be calculated by (9), assuming $\theta = \omega t$.

$$\begin{aligned} I_{INV,RMS}^2 &= \frac{1}{\pi}\int_0^{\pi} i_{INV}^2(\theta)d\theta = \frac{1}{\pi}\int_0^{\pi}\left|m\cos\theta\right|\cdot I_g^2\cos^2(\theta+\phi)d\theta \\ &= \frac{4mI_g^2}{3\pi}\cdot\cos^2\phi + \frac{2mI_g^2}{3\pi}\cdot\sin^2\phi \end{aligned} \tag{9}$$

The RMS value of the input current includes three components, DC current, the double frequency harmonic current and the high frequency harmonic current. Based on the concept of the RMS value, the RMS value of i_{INV} can also be expressed by the sum of the RMS value of its components as (10).

$$I_{INV,RMS}^2 = I_{C_F,RMS}^2 + I_{DC}^2 + I_{C_E,RMS}^2 \tag{10}$$

Ideally, all the high frequency harmonics should be filtered out by the film capacitors. Thus, the RMS value of the high frequency current is

$$\begin{aligned} I_{C_F,RMS} &= \sqrt{\frac{4mI_o^2}{3\pi}\cdot\cos^2\phi + \frac{2mI_o^2}{3\pi}\cdot\sin^2\phi - I_{DC}^2 - I_{C_E,RMS}^2} \\ &= \sqrt{\frac{4mI_o^2}{3\pi}\cdot\cos^2\phi + \frac{2mI_o^2}{3\pi}\cdot\sin^2\phi - \frac{m^2I_o^2}{4}\cos^2\phi - \frac{m^2I_o^2}{8}} \end{aligned} \tag{11}$$

The capacitance of the film capacitor can be calculated by $C = \Delta Q/\Delta V$. The voltage variation for the film capacitors should be chosen as the system requirement, which is 1% for our application. When selecting the voltage variation of the film capacitor, it should be lower than the voltage variation of the electrolytic capacitor. Because compared with double frequency, the other harmonic currents have much larger frequency. So the capacitance should be calculated by the maximum value of the coulomb go through the film capacitor. The coulomb can be calculated by

$$\begin{aligned} Q(t) &= \int i_{C_F}(t)dt = T_{on}\cdot(i_{INV}(t) - i_{INV,AVE}(t)) \\ &= \frac{d_{ab}(t)}{2}\times T_s\times[i_{INV}(t) - \int_{t_0}^{t_0+T_c} i_{INV}(t)dt] \\ &= \frac{1-d_{ab}(t)}{2}\times T_s\times[\frac{mI_o}{2}\cos\phi - \frac{mI_o}{2}\cos(2\omega t+\phi)] \qquad \omega t\in[0,\pi] \end{aligned} \tag{12}$$

Obviously, the coulomb varies with time. The equation is function of modulation index, phase angle and the power rating. The modulation index is constant if the output inverter voltage and DC-link voltage are chosen. The analytic equation of the maximum coulomb from (12) can be obtained however it's too complicated. Therefore, it's more convenient to use simulation to help calculate the maximum coulomb value by software. The relationship for 3kW maximum power and 150kHz switching frequency is plotted by Matlab as Fig. 3 where we can read the maximum coulomb value.

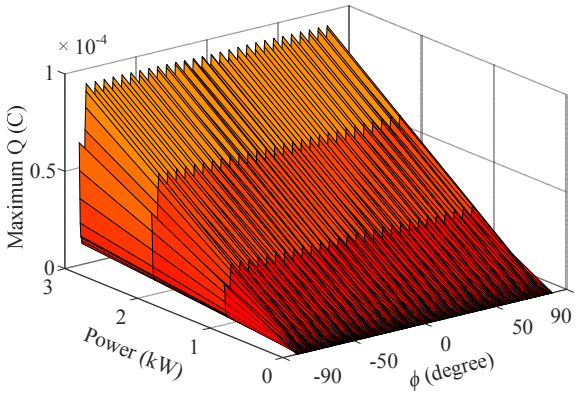

Fig. 3 Maximum Q for calculating the film capacitor.

In our case, the capacitance of the film capacitor is calculated as (13).

$$C_F = \frac{Q_{Max}}{\Delta V} = 23.1\mu F \tag{13}$$

III. Current Sharing Method for the Hybrid Capacitor Bank

Until now, the design of the electrolytic and film capacitors is completed based on the ideal case. However, the electrolytic capacitors should be oversized since some of the high frequency switching harmonic will be filtered out by them. The LC resonance filter whose resonant frequency is tuned at 120Hz can be applied for the current share in the hybrid capacitor bank. However, the drawback is that the additional inductor will increase the size of DC-bus and the voltage stress of the electrolytic capacitors. Thus, reasonable value of the inductor should be chosen.

To understand the problem, the spectra analysis of the input current i_{INV} should be deduced. The voltage harmonic for the single-phase inverters are illustrated in [11]. The input current of the three phase inverter and bipolar SPWM single-phase inverter are calculated in [12]. The input current of the inverter equals to the product of the SPWM signal and the inverter's output current which is assumed to be ideally sinusoid. Besides the double frequency harmonic, there are high frequency harmonics whose dominant frequency will be around doubled

switching frequency for unipolar SPWM modulation. Unlike the rough calculation of i_{INV} as (8), the analytical expression for input current of the single-phase inverter with unipolar SPWM modulation is shown as (17), where ω is the angular speed of the grid and ω_s represents the angular speed of switching frequency. In our case, the grid frequency is 60Hz so the double frequency harmonic is 120Hz. The switching frequency of the single-phase inverter is chosen as 150kHz. Thus, the main high frequency switching harmonics is around 300kHz.

The equivalent circuit of the hybrid capacitor bank is shown as Fig. 1. The stray resistance and inductance of the film capacitor are neglected. The stray parameters of the electrolytic are also not considered since they are negligible compared with impedance of L_E. For the convenience of the analysis, it assumes that the closed-loop controller of the DC/DC converter is ideal i_{DC} has no harmonics. In the best scenario, the double frequency current harmonic will be buffered by the electrolytic capacitor while the high frequency switching harmonics is filtered through the film capacitors. However, in reality the share of the current harmonic between the electrolytic capacitor leg and film capacitor leg depends on the ratio of their impedance. The impedance of the resonant filter and film capacitor can be expressed by (14) and (15).

$$Z_R(j\omega) = j(\omega L_E - \frac{1}{\omega C_E}) \tag{14}$$

$$Z_F(j\omega) = -\frac{j}{\omega C_F} \tag{15}$$

The current share in the resonant filter can be represented as the coefficient as (16).

$$Zc(\omega) = \frac{|Z_F(j\omega)|}{|Z_R(j\omega)|+|Z_F(j\omega)|} = \frac{C_E}{|\omega^2 C_F C_E L_E - C_F|+C_E} \tag{16}$$

The current went through the resonant filter can be expressed as (18). The RMS current in the resonant filter leg can be calculated by the sum of each component's RMS value as (19).

Based on the design of the electrolyte capacitor in previous section, LLS2V471MELB Nichicon (voltage rating: 350V; Capacitance: 470uF; Ripple current: 2.53A@120Hz) is chosen considering size and price. Two capacitors will be connected in series to match the voltage level and three strings will be connected in parallel for redundancy. The lifetime of the LLS series electrolytic capacitor can be estimated by the online tool from Nichicon. The lifetime estimation as (20) is not a guaranteed life specification but it's accurate enough for our research purpose.

$$L_n = L_0 \times 2^{\frac{T_0 - T_n}{10}} \times 2^{1-\frac{\Delta t_n}{K}} \qquad \Delta t_n = \Delta t_0 \times (\frac{I_n}{I_m})^2 \tag{20}$$

Where L_0 is the specified life time (3000 hours), T0 is the max operating temperature (85oC), T_n is the ambient temperature (chosen as 25oC), K is the Boltzmann's constant, In is the applied current and I_m is the rating current of capacitor. The frequency dependency ESR of the electrolytic capacitor results in a frequency coefficient of the ripple current RMS value. It is considered when rating the capacitor and calculating its life time. For this type of electrolytic capacitor, the frequency coefficient of 50kHz or more is 1.43. In addition, the ESL of the medium size electrolytic capacitor is from10nH to 30nH [13].

Conventionally, the inductance of the resonant filter is tuned with the 120Hz resonant frequency as (21). However, the inductor with this rating is usually quite large and costly.

$$L_{E,C} = \frac{1}{\omega^2 C_E} = 1.25mH \tag{21}$$

The impedance is plotted as The RMS ripple current and its corresponding estimated life time is plotted with different inductance selection from 10nH to 1.25mH as Fig. 5.

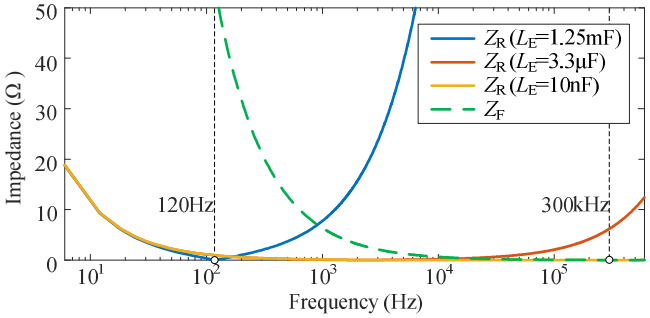

Fig. 4 Impedance of the resonant filter and film capacitor.

$$i_{INV}(t) = \frac{m}{2} I_o \cos(\phi) + \frac{m}{2} I_o \cos(2\omega t + \phi) + \sum_{j=1}^{\infty}\sum_{k=-\infty}^{\infty} \left\{ \begin{array}{l} \frac{I_o}{j\pi}\cos([j+k]\pi)\cos(\phi)\times[J_{2k+1}(jm\pi) - J_{2k-1}(jm\pi)]\cos(2j\omega_s t + 2k\omega t) + \\ \frac{I_o}{j\pi}\cos([j+k]\pi)\sin(\phi)\times[J_{2k+1}(jm\pi) + J_{2k-1}(jm\pi)]\sin(2j\omega_s t + 2k\omega t) \end{array} \right\} \tag{17}$$

$$i_E(t) = Zc(2\omega)\frac{m}{2} I_o \cos(2\omega t + \phi) + \sum_{j=1}^{\infty}\sum_{k=-\infty}^{\infty} \left\{ \begin{array}{l} \frac{I_o}{j\pi}\cos([j+k]\pi)\cos(\phi)\times Zc(2j\omega_s + 2k\omega)[J_{2k+1}(jm\pi) - J_{2k-1}(jm\pi)]\cos(2j\omega_s t + 2k\omega t) + \\ \frac{I_o}{j\pi}\cos([j+k]\pi)\sin(\phi)\times Zc(2j\omega_s + 2k\omega)[J_{2k+1}(jm\pi) + J_{2k-1}(jm\pi)]\sin(2j\omega_s t + 2k\omega t) \end{array} \right\} \tag{18}$$

$$I_{E,RMS}^2 = \left[Zc(2\omega)\frac{m}{2} I_o \right]^2 + \sum_{j=1}^{\infty}\sum_{k=-\infty}^{\infty} \left\langle \begin{array}{l} \cos([j+k]\pi)\times\left\{\frac{I_o}{j\pi}\cos(\phi)Zc(2j\omega_s + 2k\omega)[J_{2k+1}(jm\pi) - J_{2k-1}(jm\pi)]\right\}^2 + \\ \cos([j+k]\pi)\times\left\{\frac{I_o}{j\pi}\sin(\phi)Zc(2j\omega_s + 2k\omega)[J_{2k+1}(jm\pi) + J_{2k-1}(jm\pi)]\right\}^2 \end{array} \right\rangle \tag{19}$$

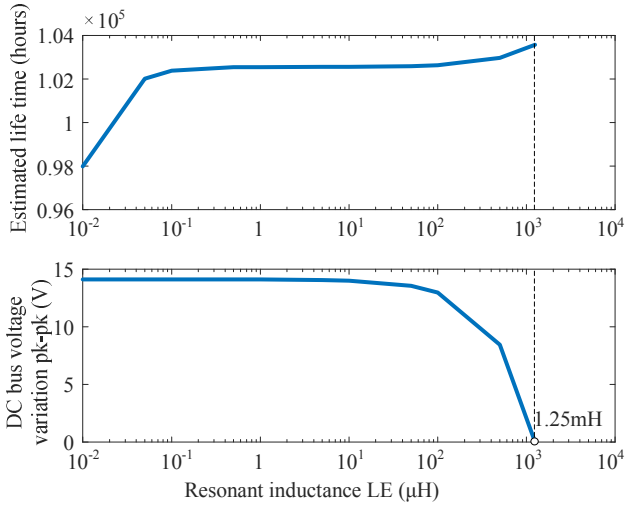

Fig. 5 Estimated lifetime of the electrolytic capacitor and DC-bus voltage variation with different resonant inductance L_E.

From Fig. 4, we can observe that the add-on inductor will increase the impedance at high frequency as 300kHz for this case. The high frequency harmonic currents tend to go through the film capacitor. So the higher L_E will result in lower RMS value of the ripple current in the electrolytic capacitors. Finally, longer life time will be achieved. From Fig. 5, we can directly observe that the electrolytic capacitor will achieve life time saving by adding the resonant inductor. But larger L_E will result in significant reduction in the DC-bus voltage variation. However, the DC-bus is already designed by the maximum allowable voltage variation. Thus the benefit of using a large L_E will not make up the disadvantage in practice. Thus, L_E is chosen as a reasonable value, like 3.3μH, resulted from the tradeoff between the lifetime saving and the size and cost of the system.

IV. Simulation and Experimental Results

The design of the hybrid capacitor bank and the current sharing method is verified by the simulation and experiment results in this section. The hybrid capacitor bank is designed for 3kW grid-tied single-phase inverter with 150kHz switching frequency. Based on the design in previous analysis, the passive components are selected by the off-the-shelf items from Digikey and Coilcraft. The design value and the selected value are listed as Table I. The manufacturer part number is also shown.

TABLE I. Passive Component Selection of the System

	Designed value	Selected value	Manufacturer Part number
C_E (mF)	0.994	1.41	LLS2V471MELB
L_E (μH)	3.3	3.3	VER2923-332KL
C_F (μF)	23.1	25	B32796E2256
L_{INV} (μH)	62.9	66	AGP4233-333
C_{INV} (μF)	4	4	B32794D2405
L_g (μH)	28.2	30	VER2923-153
R_d (Ω)	0.73	0.75	

The simulation is used to verify the current sharing with different resonant inductance value as Fig. 8. The simulation model is built by Matlab/Simulink. From the simulation results, we can see that the RMS value of the current going through the electrolytic capacitors reduces significantly by adding an inductor in series with the capacitor to form a resonant filter. In this way, the life time of the electrolytic capacitor can be saved. Moreover, the most current reduction can be achieved by designing the inductor at the resonant frequency, 1.25mH while the RMS value can be reduced significantly by adding a reasonably small inductance, like 3.3μH. We make the following conclusions that in terms of life time saving for the electrolytic capacitor: (1) It's practical to design the capacitor bank as a hybrid capacitor bank which combines electrolytic capacitors and film capacitors; (2) Adding an small value of inductor in series with the electrolytic capacitor to form a resonant filter will further extend the life time of the electrolytic capacitor. Additionally, since the ESR value of the electrolytic capacitor is relatively large, the reduction of the RMS value of the current will result in the power loss reduction of the system.

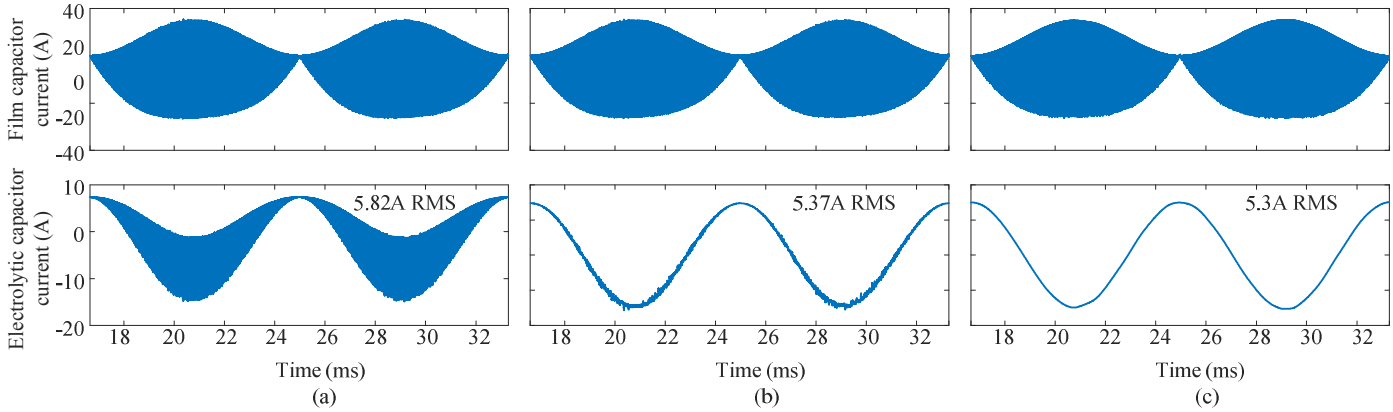

Fig. 6 Current sharing performance: (a) L_E =10nH; (b) L_E =3.3uH; (c) L_E =1.25mH.

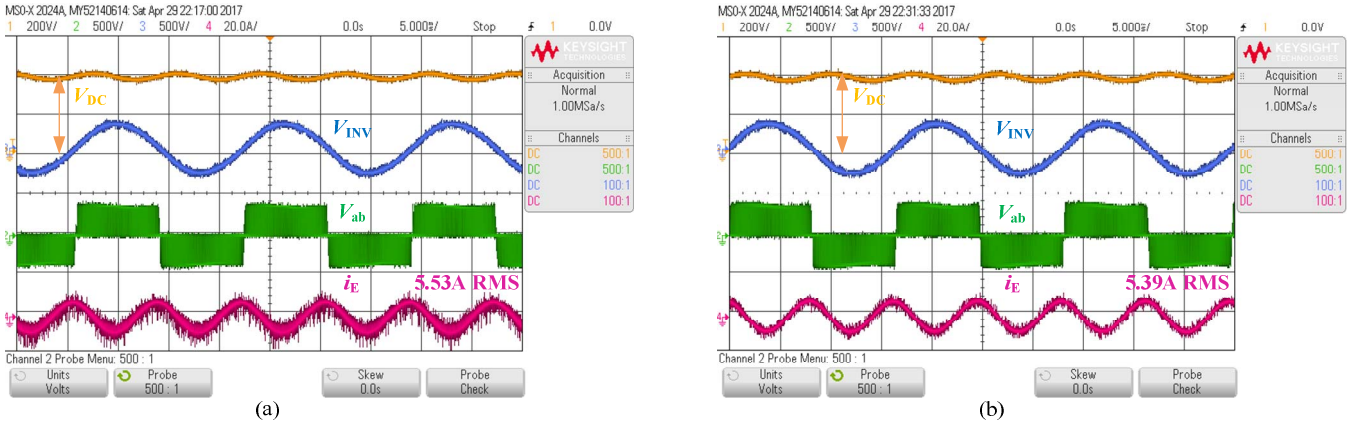

Fig. 7 Experimental verification of the current sharing method: (a) no add-on L_E; (b) L_E =3.3uH.

The experiment setup is shown as Fig. 8 where the LCL single-phase inverter passive-damping is built. The full bridge inverter is controlled by the TI DSP28377D microcontroller. The experimental results showed as Fig. 7 also verify the current sharing method. The RMS value i_E is reduced from 5.53A to 5.39A by adding a 3.3μH inductor in series with the electrolytic capacitor. It should be noted that the benchmark experiment as Fig. 7 (a) is done by replace the 3.3μH with a wire. This wire will also add some stray inductance to the electrolytic capacitor thus its RMS value is lower than the simulation results as Fig. 6 (a) which is ideal condition.

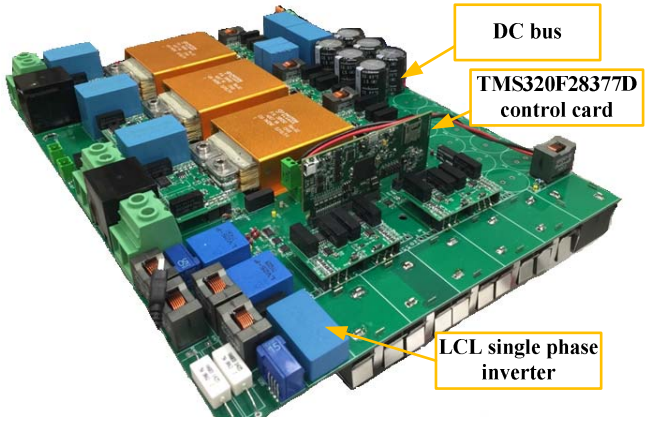

Fig. 8 Experiment setup.

V. Conclusions

A hybrid capacitor bank is designed and utilized in the DC-bus of the single-phase inverter system. The hybrid capacitor bank is composed by the LC resonant filter with electrolytic capacitor and film capacitor. The design procedure of the hybrid capacitor bank for the single-phase inverter with unipolar modulation is discussed. The performance of the proposed capacitor bank is verified by both simulation and experimental results.

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