

An Isolated High-Voltage High-Frequency Pulsed Power Converter for Non-Thermal Plasma Ozone Generation

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Abstract— An isolated high-voltage high-frequency pulsed power converter for non-thermal plasma ozone generation is proposed in this paper. With an input of 500 VDC, the output pulsed voltage can reach -12 kV through the inductor-capacitor resonance together with a step-up transformer. The pulse duration is designed as 1.66 μ s. An anti-series connected switch pair at the input terminal enables the energy stored in the passive component to be recovered and transferred back to the DC source which results in great energy saving. A hardware prototype with 500 VDC input and -12 kV pulsed voltage output has been developed. The pulse generating frequency can go up to 15 kHz. Both the simulation and experimental results are presented to validate the proposed pulsed power converter and its operating principle.

I. INTRODUCTION

Pulsed power generation is a promising technology with various and broad applications. The output voltage/current employs various shapes, amplitudes, durations (pulse widths), and pulse frequencies depending on various load requirements. The applications of such pulsed power supplies lie in extensively diverse areas. For instance, the ionization process, material joining, electron beam generation, concrete recycling, wastewater processing, radar, plasma, etc [1]. With the fast-growing demands for pulsed power in the food industry, water industry, and materials fabrication, pulsed power generation technology is receiving increasing attention in recent decades. The technologies for generating high pulsed power can be classified into four categories: magnetic pulse compressors, multistage Blumlein lines, hard tube pulsers and solid state switching circuits. With the exception of solid state switching circuits, all of these technologies utilize either spark gaps or vacuum tubes as high voltage switches, which makes

them bulky and inefficient [1]. Thus, the scope of this paper has been focused on solid state switching circuits.

Among the application areas mentioned above, plasma systems are currently the most substantial application of pulsed power technology [2]. Fig. 1 is a conceptual drawing for the plasma reactor chamber. Ozone has been widely used in water treatment, food sterilization, chemical synthesis, bleaching processes, etc. That said, the production, storage and transportation of ozone involves potential safety hazards; therefore, ozone is generated where it is needed in most circumstances [3]. Different types of plasma discharge for ozone generation have been studied and utilized [4]-[6], among which non-thermal plasma discharge incorporates several merits compared to its counterparts. The primary advantage of using non-thermal discharge is that a large portion of the electric energy is saved by only motivating the electrons without heating air molecules and electrodes. The large-gradient pulse voltage has an efficiency which is 20% higher than that of the continuous waveform power supply [1]. Also, the atmospheric pressure is suitable for plasma generation. The elimination of the dielectric barrier offers higher reliability and allows for less thermal decomposition of

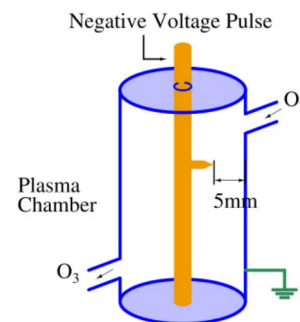


Figure 1. Conceptual drawing of a plasma reactor chamber.

ozone [7]. The pulsed power supply is a crucial part of non-thermal plasma systems, which determines the ozone generation rate, output stability, volume, and the lifetime of the system. The requirements for the pulsed power supply include high efficiency, high power density, low weight, high reliability, and stability. A conventional topology for the pulsed power converter is the Marx or Marx-oriented topologies [8]-[10], which is shown in Fig. 2.

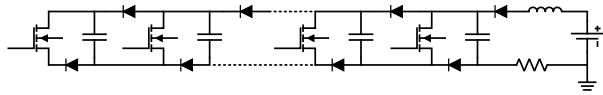


Figure 2. Marx topology

The basic idea is to cascade multiple switch-capacitor-diode units to boost the output voltage. The disadvantage of such an approach is that a large number of semiconductor devices are required to generate high pulsed voltage which would impact the system reliability. The high switching loss would also harm the system efficiency. Also for Marx topologies, high pulse frequency can hardly reach as high as 15kHz.

An isolated single-ended resonant topology controlled by DSP, shown in Fig. 3, is proposed in this paper to convert DC to high frequency high voltage pulsed power. The pulse frequency range is 500 Hz to 15 kHz. The input DC voltage is 500 V and the output pulsed voltage is rated at -12 kV. Pulse duration is 1.6 μ s. The rest of the paper is organized as follows: Section II introduces the topology and operating principle of the proposed pulsed power converter. Section III provides the simulation verification. Section IV shows the hardware setup and the experimental results which validate the proposed topology. Section V concludes the paper.

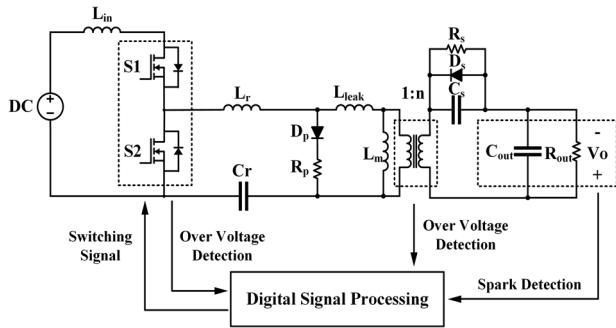


Figure 3: Proposed DC to high-pulsed-power converter

II. PULSED POWER CONVERTER OPERATING PRINCIPLE

The operation of the pulsed power converter is composed of 4 modes as shown in Fig. 4 (a) to (d). Fig. 5 is the corresponding waveforms of the input current, resonant inductor current, resonant capacitor voltage and the output pulsed voltage.

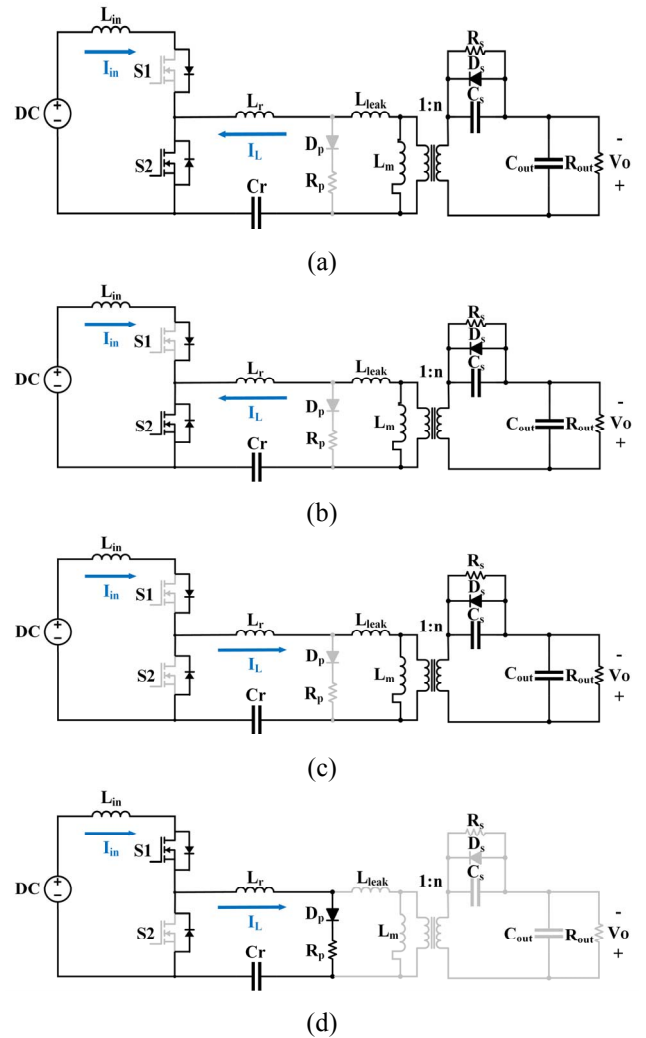


Figure 4(a)-(d). Equivalent circuits for converter operating mode 1-4

A. Mode 1

In Mode 1 (t_0-t_1), switch S_1 is off and S_2 is on. It should be noted that the resonant capacitor C_r has already been charged to its maximum value V_{cr_max} before S_2 is on. At the moment when S_2 is on, a resonant loop is formed which includes the resonant inductor L_r , transformer leakage inductance L_{leak} , resonant capacitor C_r , and the reflected capacitance from the load. The transformer magnetizing inductance L_m and capacitance C_s is large enough to be excluded from the resonance. The waveform of the inductor current through L_r is sinusoidal because of the resonance. The duration of Mode 1 is calculated in (1).

$$t_1 - t_0 = \pi \sqrt{(L_r + L_{leak}) \left(\frac{C_r \cdot C_0 \cdot n^2}{C_r + C_0 \cdot n^2} \right)} \quad (1)$$

B. Mode 2

In Mode 2 (t_1-t_2), the current through L_r is reversed and continues to flow through the body diode of the switch or the external anti-parallel diode. The resonant capacitor C_r finished discharging at the end of Mode 2.

The voltage equations for duration of mode1 and mode2 can be summarized as (2) to (4).

$$iL_r + \frac{VC_r}{R_o/n^2} = (-C_o \cdot n^2) \cdot \frac{dV_{tr}}{dt} \quad (2)$$

$$VL_r + VL_{leak} = (L_r + L_{leak}) \cdot \frac{diL_r}{dt} \quad (3)$$

$$iL_r = (-C_r) \cdot \frac{dVC_r}{dt} \quad (4)$$

Where VL_r , VL_{leak} , VC_r and V_{tr} are the voltages across the resonant inductor, leakage inductor, resonant capacitor and the transformer primary winding. iL_r is the resonant inductor current. With the maximum resonant capacitor voltage VC_{r_max} , the resonant inductor current iL_r , the transformer primary voltage V_{tr} and the output voltage V_o and can be approximately derived in (5) to (7) respectively.

$$iL_r \approx \frac{\sqrt{C_o \cdot n^2 \cdot C_r \cdot (L_r + L_{leak}) \cdot (C_o \cdot n^2 + C_r)}}{L_r \cdot (C_o \cdot n^2 + C_r)} \cdot VC_{r_max} \sin\left(\frac{\pi}{t_1 - t_0} t\right) \quad (5)$$

$$V_{tr} \approx \frac{C_r}{C_o \cdot n^2 + C_r} \cdot VC_{r_max} \cdot (\cos\left(\frac{\pi}{t_1 - t_0} t\right) - 1) \quad (6)$$

$$V_o \approx n \cdot \frac{C_r}{C_o \cdot n^2 + C_r} \cdot VC_{r_max} \cdot (\cos\left(\frac{\pi}{t_1 - t_0} t\right) - 1) \quad (7)$$

C. Mode 3

In Mode 3 (t_2-t_3), the voltage across the resonant capacitor C_r reaches its minimum value VC_{r_min} . Switch S_1 is on and S_2 is off. The DC source charges the resonant capacitor along the input inductor L_{in} and resonant inductor L_r . The transformer primary winding is shunted by the fast recovery diode D_p and ballast resistor R_p , which will eliminate the positive voltage oscillation across the transformer and balance the output voltage from negative value to a small positive value.

The duration of Mode 3 is calculated in (8).

$$t_3 - t_2 = \sqrt{(L_{in} + L_r) C_r} \cdot (\pi - \varphi) \quad (9)$$

Where φ equals to:

$$\varphi = \arccos\left(\frac{(VDC - VC_{r_min}) \cdot \sqrt{(L_{in} + L_r) C_r}}{L_{in} + L_r}\right) \quad (10)$$

$$\sqrt{(VDC - VC_{r_min})^2 \cdot \frac{C_r}{L_{in} + L_r} + \frac{VDC^2 \cdot (t_2 - t_0)^2}{L_{in}^2}}$$

The voltage equations can be summarized as (10) to (14).

$$VDC - VL_{in} - VL_r - VR_p - VC_r = 0 \quad (10)$$

$$VL_{in} = L_{in} \cdot \frac{diL_{in}}{dt} \quad (11)$$

$$VL_r = L_r \cdot \frac{diL_r}{dt} \quad (12)$$

$$VR_p = R_p \cdot iL_{in} \quad (13)$$

$$iL_{in} = C_r \cdot \frac{dVC_r}{dt} \quad (14)$$

Where VDC , VL_{in} and VR_p are the voltages across the DC source, input inductor and the ballast resistor. iL_{in} is the resonant inductor current. With the minimum resonant capacitor voltage VC_{r_min} , the input charging current iL_{in} and the resonant capacitor voltage VC_r can be derived in (15) and (16) respectively.

$$iL_{in} \approx (VDC - VC_{r_min}) \cdot \frac{\sqrt{(L_{in} + L_r) \cdot C_r}}{L_{in} + L_r} \cdot \sin\left(\frac{1}{\sqrt{(L_{in} + L_r) \cdot C_r}} t\right) + \left(\frac{VDC \cdot (t_2 - t_0)}{L_{in}}\right) \cdot \cos\left(\frac{1}{\sqrt{(L_{in} + L_r) \cdot C_r}} t\right) \quad (15)$$

$$VC_r \approx (VC_{r_min} - VDC) \cdot \cos\left(\frac{1}{\sqrt{(L_{in} + L_r) \cdot C_r}} t\right) + VDC + \left(\frac{VDC \cdot (t_2 - t_0)}{L_{in}}\right) \cdot \frac{\sqrt{(L_{in} + L_r) \cdot C_r}}{C_r} \cdot \sin\left(\frac{1}{\sqrt{(L_{in} + L_r) \cdot C_r}} t\right) \quad (16)$$

The maximum resonant capacitor voltage is obtained by equating the input charging current iL_{in} to 0 as (17):

$$VC_{r_max} = \left|_{t=t_3-t_2} VDC + \sqrt{\frac{VDC^2 \cdot (t_2 - t_0)^2}{L_{in}^2} \cdot \frac{L_{in} + L_r}{C_r} + (VC_{r_min} - VDC)^2} \quad (17)$$

where VC_{r_min} is:

$$VC_{r_min} = \sqrt{VC_{r_max}^2 - \frac{2 \cdot P_{out}}{f_{operation}}} \quad (18)$$

$f_{operation}$ varies from 500 Hz to 15kHz.

The main charging loop is composed of inductor, capacitor and resistor in series connection. The damping factor ζ in this RLC circuit is defined in (20):

$$\zeta = \frac{R_p}{2} \sqrt{\frac{C_r}{L_{in} + L_r}} \quad (20)$$

For this topology, in order to minimize the conduction loss of ballast resistor R_p , the value of R_p should be less than a threshold value making the damping factor ζ much smaller than 1. The RLC charging circuit functions at non-damped operation as:

$$R_p < R_{p_threshold} \ll 2 \sqrt{\frac{L_{in} + L_r}{C_r}} \quad (21)$$

Because of the existence of capacitor C_s , after mode 2, the voltage on the output capacitor will not get back to zero fast enough which is not preferred in this design. Ballast resistor R_p is used to balance voltage on the output capacitor, by

forcing the charging current flows to output capacitor, making the output voltage fall to zero faster.

D. Mode 4

In Mode 4 (t_3-t_4), both switch S_1 and S_2 are off, there is no current flowing in the circuit. The voltage on the resonant capacitor remains at its maximum value VC_{r_max} . The requirement for the resonant period can be written as follows in respect to the pulse frequency range from 500 Hz to 15 kHz. The minimum pulse interval, which is 67 μ s, should be longer than one operation period from t_0 to t_3 , as shown in (22)

$$t_3-t_0=2\pi\sqrt{(L_r+L_{leak})\left(\frac{C_o n^2 C_r}{C_o n^2+C_r}\right)+\sqrt{(L_{in}+L_r)\cdot C_r}\cdot(\pi-\varphi)}<67\ \mu\text{s} \quad (22)$$

Where φ equals to:

$$\varphi=\arccos\left(\frac{(VDC-VC_{r_min})\cdot\sqrt{(L_{in}+L_r)C_r}}{\sqrt{(VDC-VC_{r_min})^2\cdot\frac{C_r}{L_{in}+L_r}+\frac{VDC^2\cdot(t_2-t_0)^2}{L_{in}^2}}}\right)$$

Fig. 5 is the corresponding waveforms of the input current, resonant inductor current, resonant capacitor voltage and the output pulsed voltage from mode 1 to mode 4.

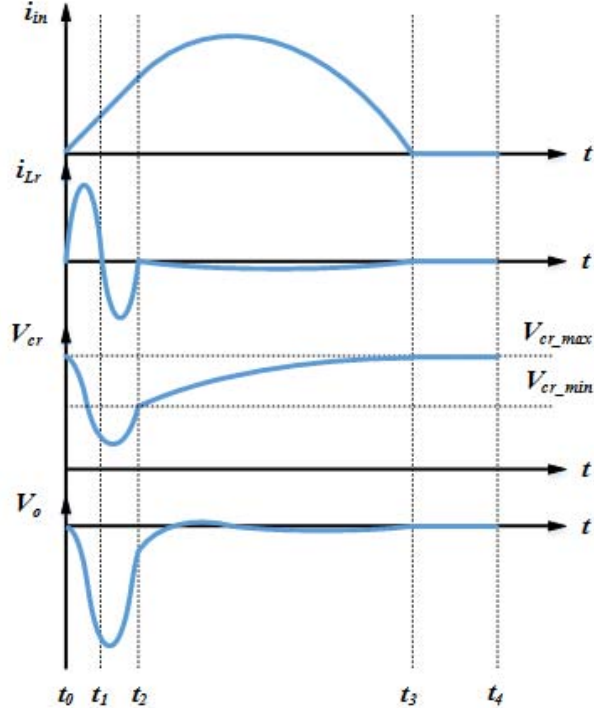


Figure 5. Principle operating waveforms.

III. SIMULATION VERIFICATION

A simulation model of the pulsed power converter has been developed in PSIM. The converter specifications and the calculated parameters are listed in Table I. Fig. 6 shows the simulation waveforms. The zoomed-out waveforms of the gating signal, input charging current, primary side resonant current and the output pulsed voltage are shown in Fig.6 (a). The zoomed-in waveforms are shown in Fig. 6 (b).

Based on (1), pulse duration is:

$$t_pulse=2\cdot(t_2-t_0)=1.6\ \mu\text{s}$$

Which is verified in Fig. 6(b).

TABLE I. SIMULATION MODEL PARAMETERS

Parameter	Value
DC input voltage	500 V
Pulsed voltage	-12 kV
Input inductor	0.8 mH
Resonant inductor	0.55 μ H
Resonant capacitor	200 nF
Transformer turn ratio	1:18

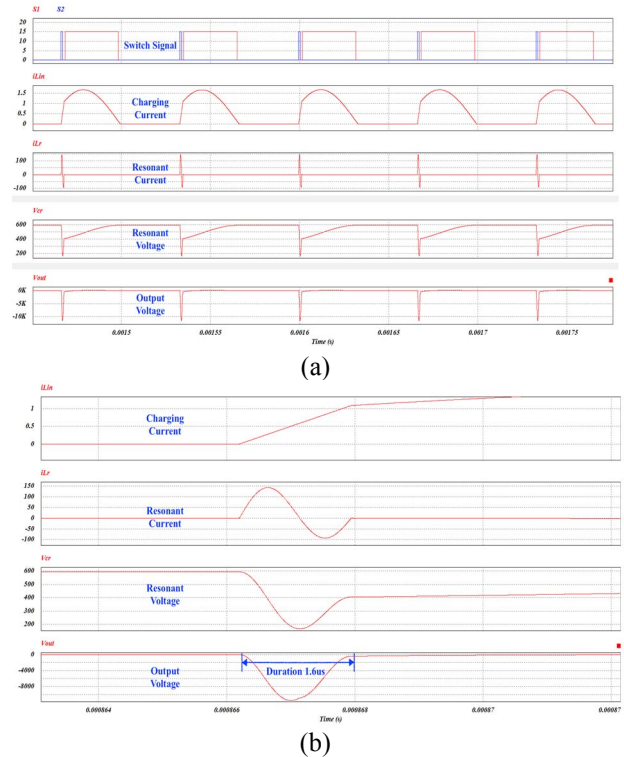


Figure 6. Simulation waveforms of gating signal, primary side resonant current and the output pulsed voltage. (a) zoomed-out waveforms; (b) zoomed-in waveforms

IV. EXPERIMENTAL VERIFICATION

The transformer is the core part in this design for the sake of a stable and efficient operation. A ferrite toroidal core of 50 mm×30 mm×20 mm is selected. The primary has 6 turns and the peak AC flux density is 157 mT.

The number of turns for secondary winding is 108. The windings must be arranged in a way that the leakage inductance and stray capacitance are minimized in order to improve the high frequency response. The total primary inductance is 180 μH and the leakage inductance is 0.6 μH in this design. Progressive winding method has been used to reduce the stray capacitance. A transformer model developed in ANSYS/Maxwell, shown in Fig. 7, verifies the design. The total insulation thickness of fiber glass tape between the primary and secondary is 2.5 mm, with insulating ability up to 25 kV. The external surface is immersed with epoxy resin under vacuum environment.

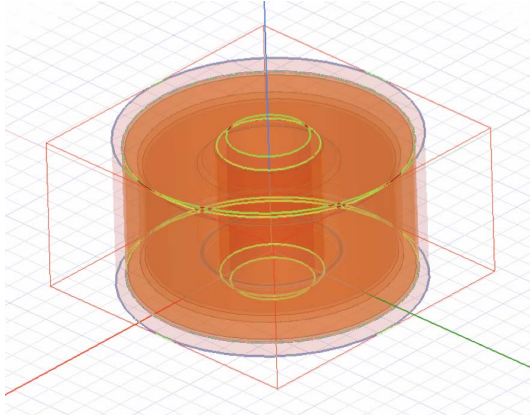


Figure 7. Transformer model in ANSYS/Maxwell

In this paper, the resonant capacitor is selected as 200nF, the output capacitor is 280 pF, and the leakage inductance of transformer is 0.6 μH. The pulse duration is designed at 1.6 μs. Based on (23), resonant inductor's value is obtained by:

$$L_r = \frac{\text{Pulse duration}^2}{\left(\frac{C_r \cdot C_o \cdot n^2}{C_r + C_o \cdot n^2}\right) \cdot 4\pi^2} - L_{leak}$$

$$= \frac{1.6 \mu\text{s}^2}{\left(\frac{200 \text{ nF} \cdot 280 \text{ pF} \cdot 18^2}{200 \text{ nF} + 280 \text{ pF} \cdot 18^2}\right) \cdot 4\pi^2} - 0.6 \mu\text{H} = 0.55 \mu\text{H} \quad (23)$$

The input inductor is 0.8 mH, which makes operation duration t_3-t_0 is less than 67 μs.

Ballast resistor will influence the overall efficiency, positive ripple voltage of output capacitor and the speed of output voltage falling back to zero. Thus, the selection of the ballast resistor needs considering all the three factors above. As this paper mentioned as (21), ballast resistor's value needs less than a threshold value. In this paper, $R_{p_threshold}$ is set

as 20Ω. In this case, damping factor ζ of RLC charging circuit is less than 0.15. The charging loop functions at the non-damped operation:

$$\zeta < \zeta_{\text{threshold}} = \frac{R_{p_threshold}}{2} \sqrt{\frac{C_r}{L_m + L_r}} = \frac{20}{2} \cdot \sqrt{\frac{200 \text{ nF}}{0.55 \mu\text{H} + 0.8 \text{ mH}}} = 0.15 \quad (24)$$

Different values of ballast resistor have been compared and tested. Results consisting of power loss P_{Rp_loss} for ballast resistor, positive ripple voltage V_{ripple} on output capacitor and settle time t_s for duration of output voltage getting back to zero are listed in Table II. By comparison, resistance of ballast resistor is selected as 8 Ω.

TABLE II. BALLAST RESISTOR SELECTION

R_p (Ω)	P_{Rp_loss} (w)	V_{ripple} (V)	t_s (μs)
5	3.5635	76	9.65
8	7.9	134	6.73
11	9.594	190	5.08
14	10.86	240	3.77

Fig. 8 is the hardware prototype that has been developed and tested to full voltage rating. Two IGBTs were used for S_2 with the current sharing purpose. The experimental waveforms are shown in Fig. 9. It can be seen from Fig. 8 that the output pulsed voltage reaches 12 kV with a pulse duration of 1.6 μs. Although the IGBTs for S_2 are turned off after the channel current turns to zero, the collector-emitter voltage still sees a voltage spike when the IGBTs stop conducting current. In addition, the current ringing occurs when the resonant current reaches zero. It is mainly caused by the diode reverse recovery loss. A feasible solution would be utilizing the SiC diodes in anti-parallel connection with the IGBTs.

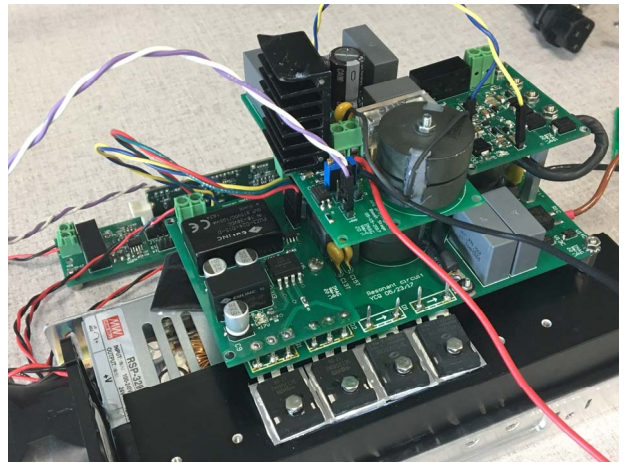


Figure 8. Pulsed power converter prototype

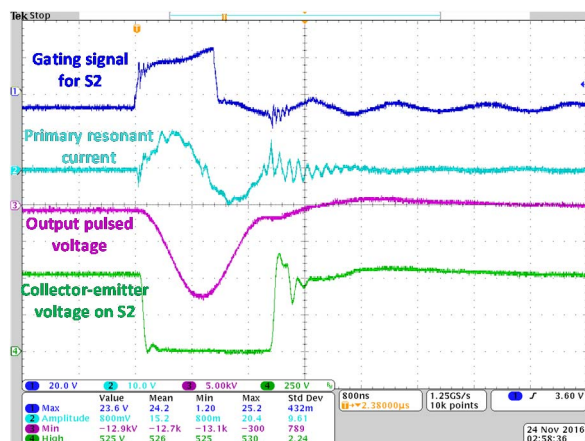


Figure 9. Measured waveforms of gating signal, primary resonant current, output pulsed voltage and the IGBT collector-emitter voltage.

V. CONCLUSION

A high voltage high frequency pulsed power converter has been proposed in this paper. The major application of the proposed converter is for non-thermal plasma ozone generation. A detailed analysis for the converter operating principle and parameter calculation has been provided. Both a simulation model and a hardware prototype have been developed. The output pulsed voltage can reach -12 kV with 500 VDC input. The pulse generating frequency can go up to 15 kHz. The proposed converter and its operating principle have been well validated.

ACKNOWLEDGMENT

The authors would like to thank Mr. Xiaohang Yu for his valuable input and suggestions.

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